

MODEL NAME : *KML50*
PCB NO : *LA-4596P (DA60000B710)*
BOM P/N : *11*

Half Penny Bridge 15.4

Compal Confidential

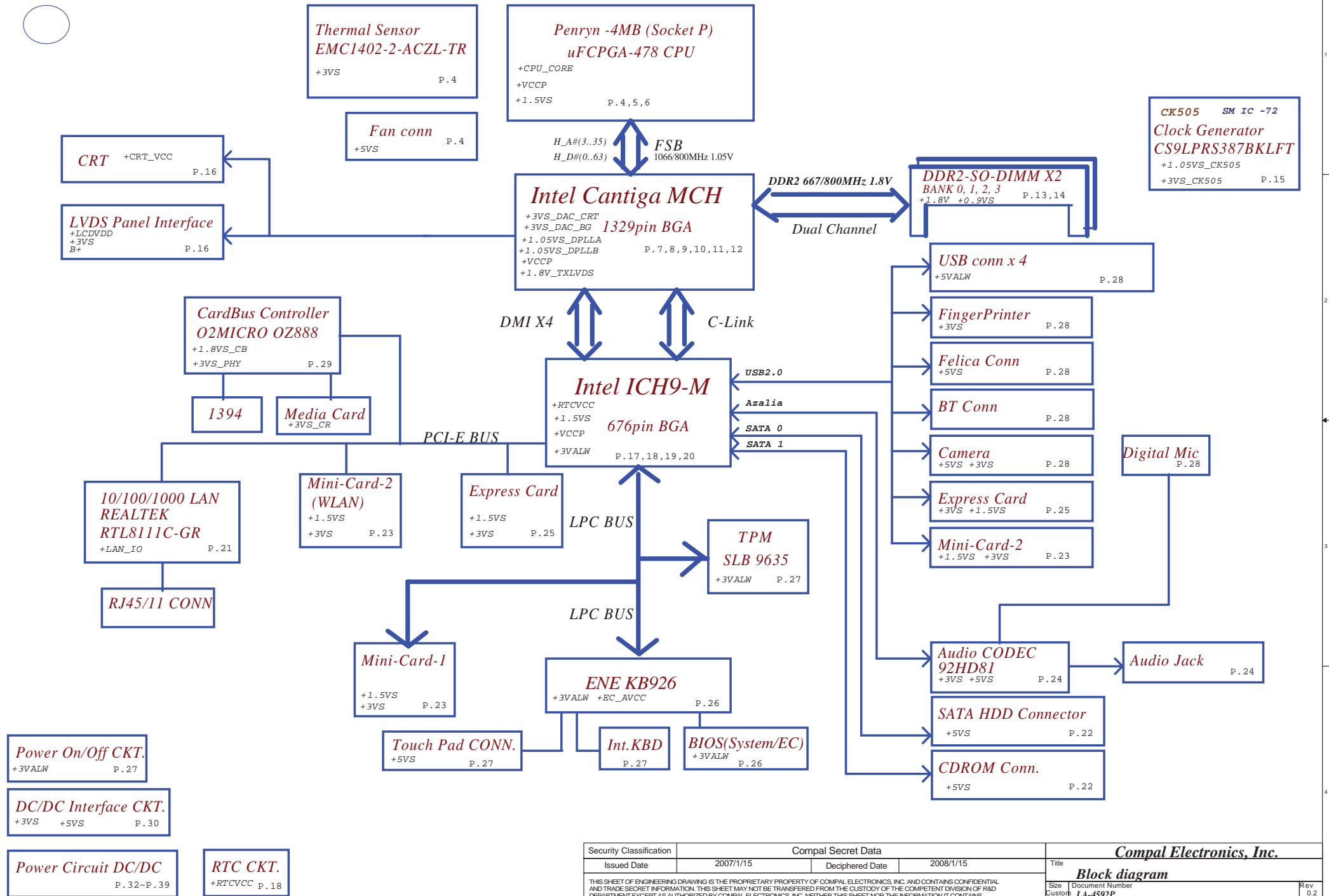
Schematic Document

Cantiga + ICH9

2009 / 01 / 14 Rev:1.0(A00)

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				Date: Thursday, February 19, 2009	Rev 0.2
				Sheet 1 of 43	

Half Penny Bridge 15.4



power plane State	+B	+5VALW +3VALW	+1.8V	+5VS +3VS +1.5VS +0.9V +VCCP +CPU_CORE +1.8VS
S0	O	O	O	O
S1	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

ICH9-M	USB PORT#	DESTINATION
	0	JUSBP1
	1	CAMERA
	2	JUSBP3
	3	Felica
	4	Blue Tooth
	5	Finger Printer
	6	JMINI2-WLAN
	7	Express card
	8	JUSBP3
	9	JMINI1-WWAN
	10	JUSBP4
	11	NA

I2C / SMBUS ADDRESSING

DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	1 0 1 0 0 0 0
DDR SO-DIMM 1	A4	1 0 1 0 0 1 0
CLOCK GENERATOR (EXT.)	D2	1 1 0 1 0 0 1 0

Symbol Note :



: means Digital Ground



: means Analog Ground

@ : means just reserve , no build

CONN@ : means ME CONN compont.

TPM@:TPM compont

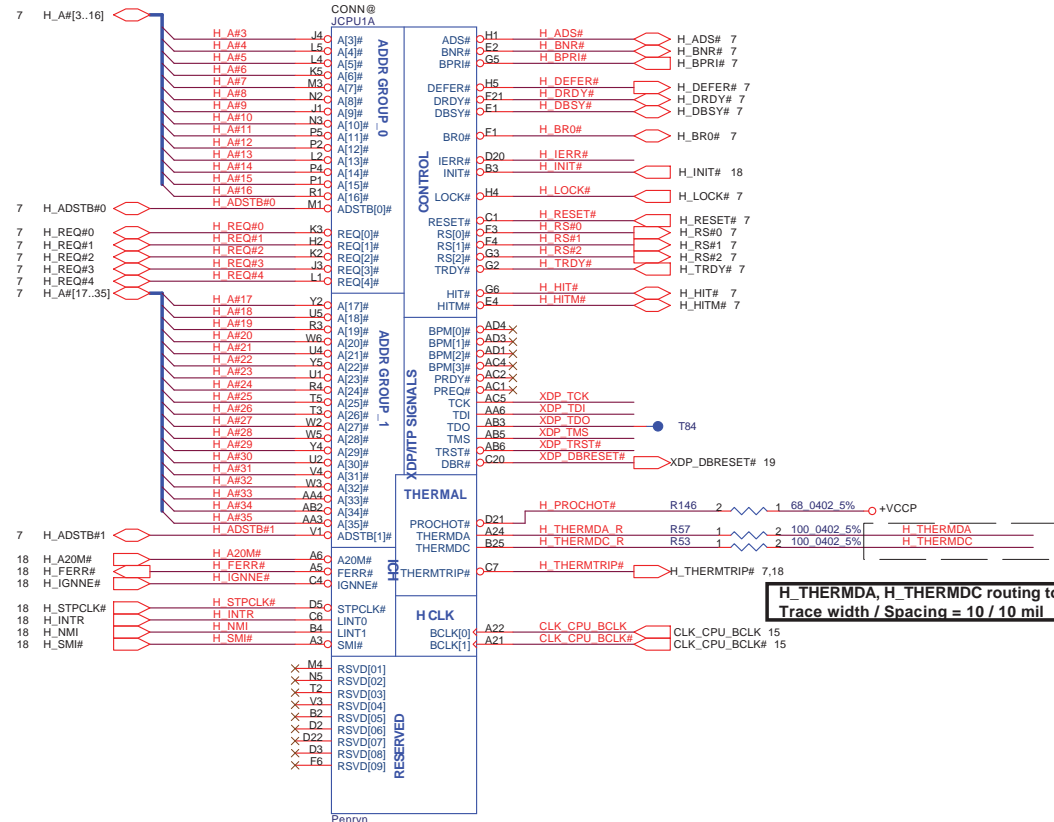
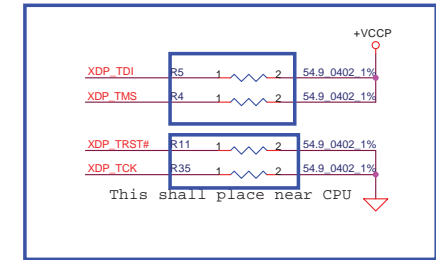
PCI EXPRESS	DESTINATION
Lane 1	MINI CARD-1 WWAN
Lane 2	GLAN RTL8111DL
Lane 3	MINI CARD-2 WLAN
Lane 4	EXPRESS CARD
Lane 5	CARD READER OZ888
Lane 6	NA

SATA	DESTINATION
Lane 0	HDD
Lane 1	ODD
Lane 4	NA
Lane 5	NA

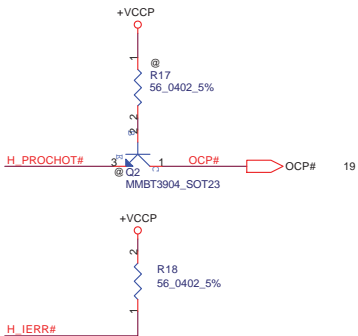
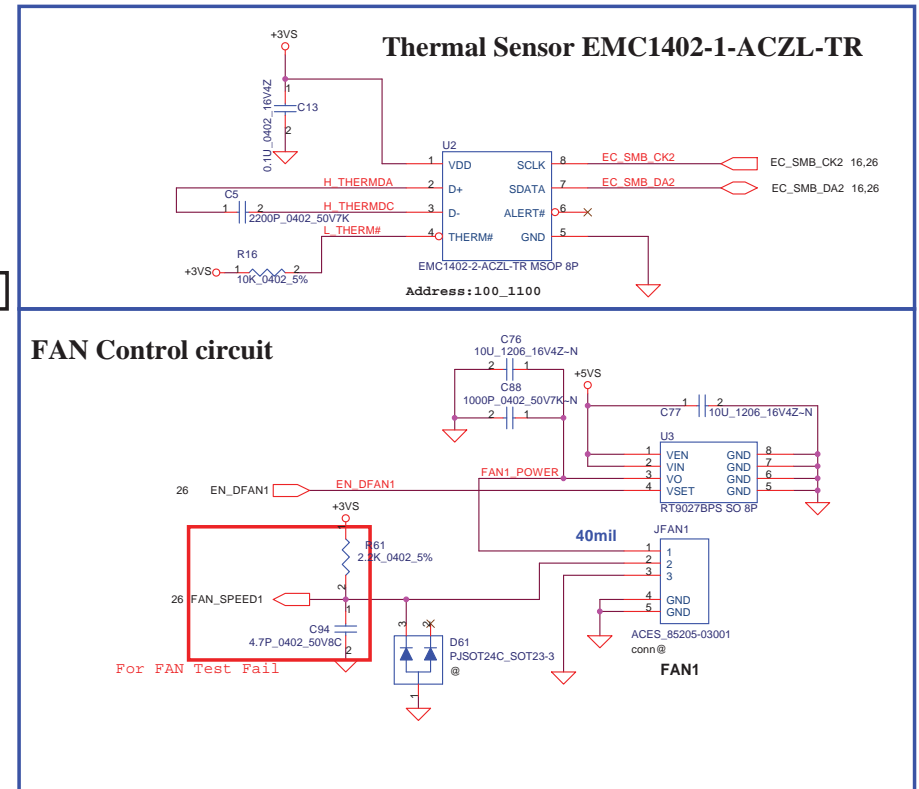
SMBUS Control Table

	SOURCE	INVERTER	BATT	SERIAL EEPROM	THERMAL SENSOR (CPU)	SODIMM	CLK CHIP	MINI CARD	LCD
SMB_EC_CK1 SMB_EC_DA1	KB926	X	V	V	X	X	X	X	X
SMB_EC_CK2 SMB_EC_DA2	KB926	X	X	X	V	X	X	X	X
SMB_CK_CLK1 SMB_CK_DAT1	ICH9	X	X	X	X	V	V	V	X
LCD_CLK LCD_DAT	Cantiga	X	X	X	X	X	X	X	V

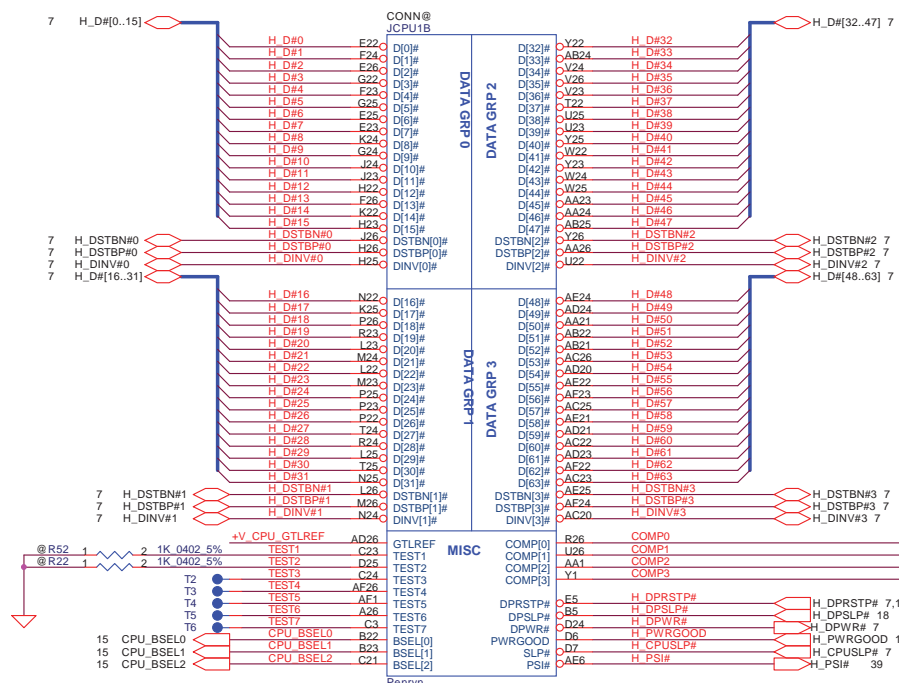
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				Custom	LA-4592P	0.2
				Date:	Thursday, February 19, 2009	Sheet 3 of 43



H_THERMDA, H_THERMDC routing together,
Trace width / Spacing = 10 / 10 mil



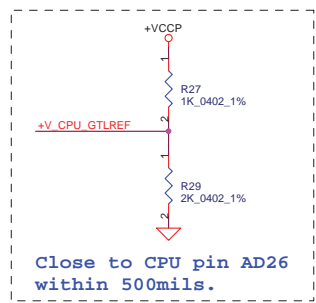
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Size	Document Number	Date		Rev	
Custom	LA-4592P	Thursday, February 19, 2009		0.2	
Sheet		4		of	
43					



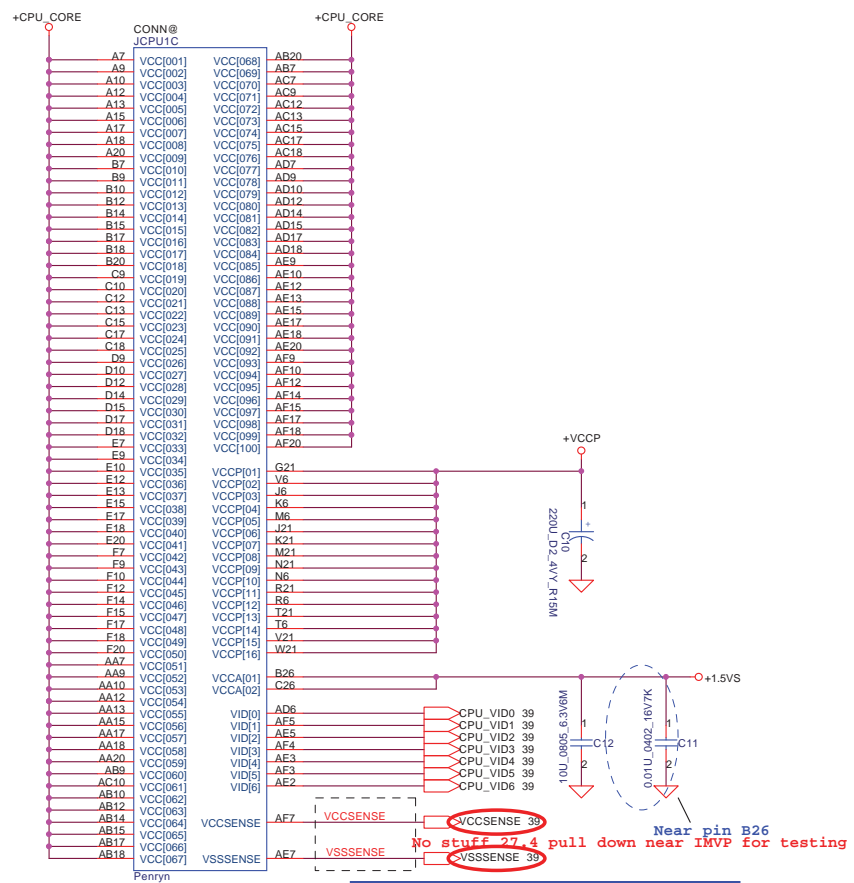
layout note: Rout H_DPRSTP# from ICH9 to IMPV6 then to GMCH & CPU

layout note: Route TEST3 & TEST5 traces on ground referenced layer to the TPs

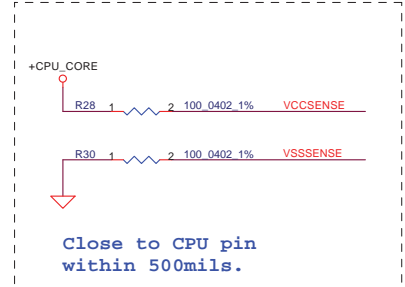
Resistor placed within 0.5" of CPU pin. Trace should be at least 25 mils away from any other toggling signal. COMP[0,2] trace width is 18 mils. COMP[1,3] trace width is 4



For 6 layer
Z=27.4 ohm
VCCSENSE, VSSSENSE/ 14mils (MS),
16mils (SL) width, 7mils space, 25mils
space to other signals Mismatch =25mils.



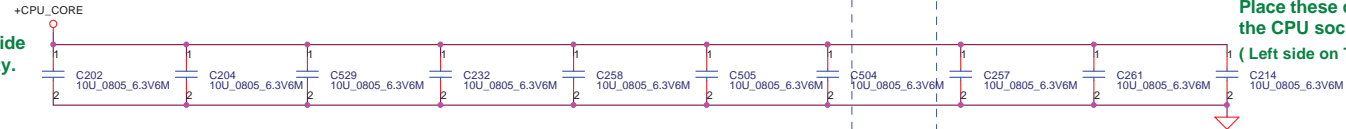
Length match within 25 mils.
The trace width/space/other is 20/7/25.



High Frequency Decoupling

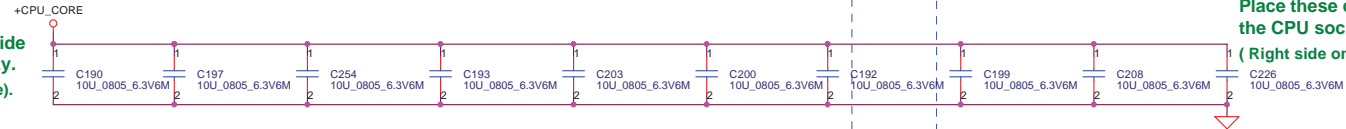
10uF 0805 X5R -> 85 degree.

Place these caps inside the CPU socket cavity. (Left side on Top).



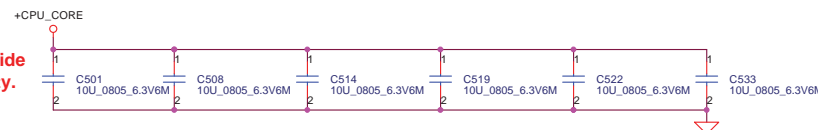
Place these caps inside the CPU socket. (Left side on Top).

Place these caps inside the CPU socket cavity. (Right side on Top side).

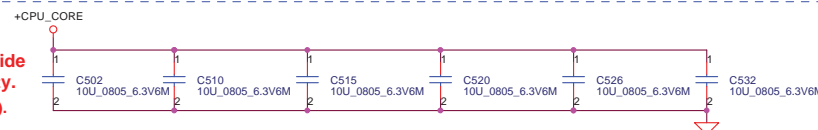


Place these caps inside the CPU socket. (Right side on Top).

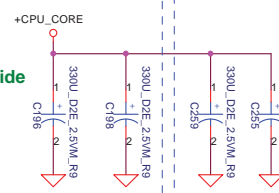
Place these caps inside the CPU socket cavity. (Left side on Bottom).



Place these caps inside the CPU socket cavity. (Right side on Bottom).



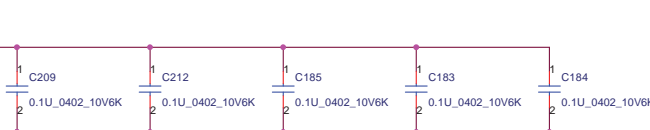
Place these caps inside the CPU socket. (Left side on Top).



Place these caps inside the CPU socket. (Right side on Top side).

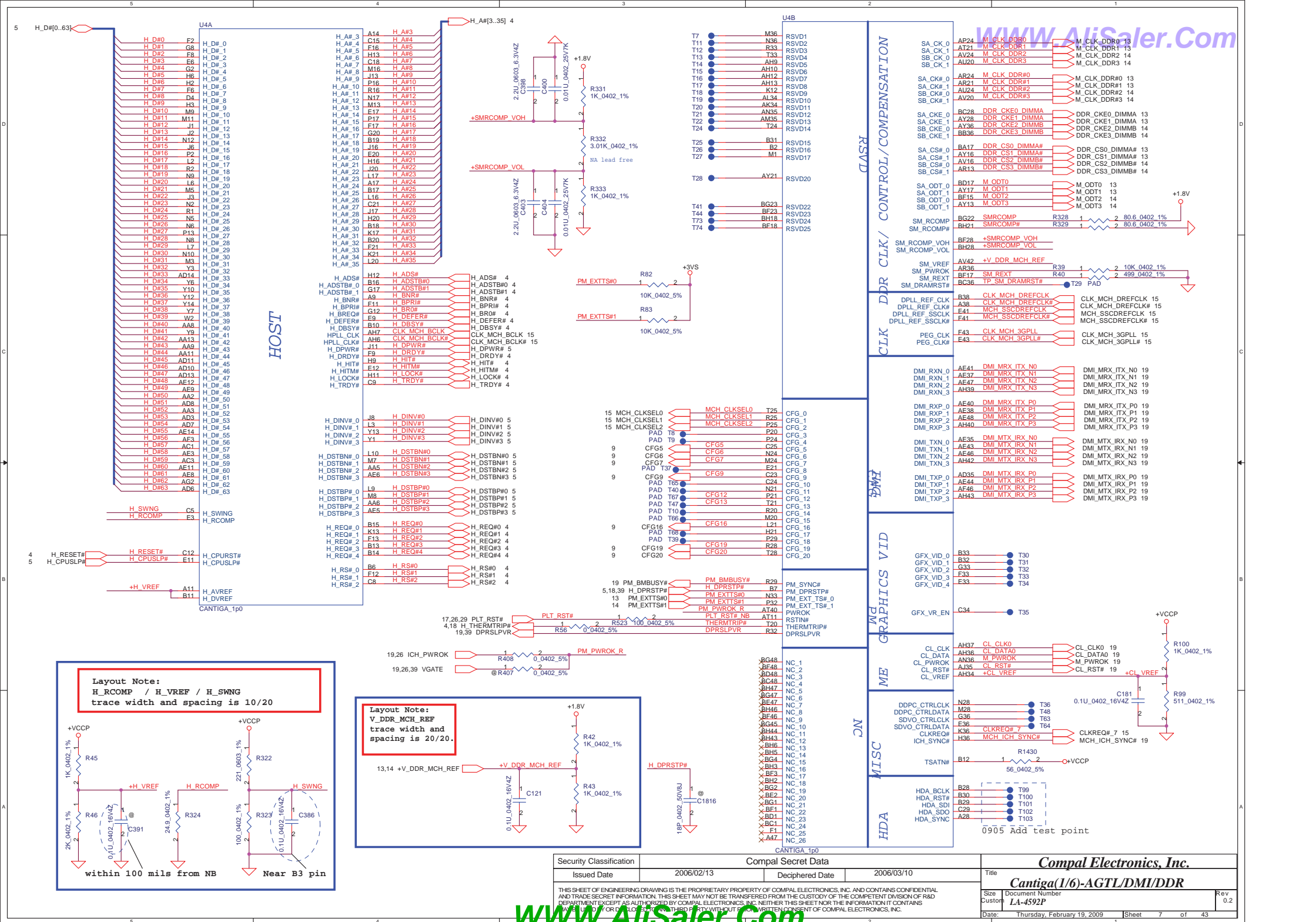
ESR <= 1.5m ohm
Capacitor > 880 uF

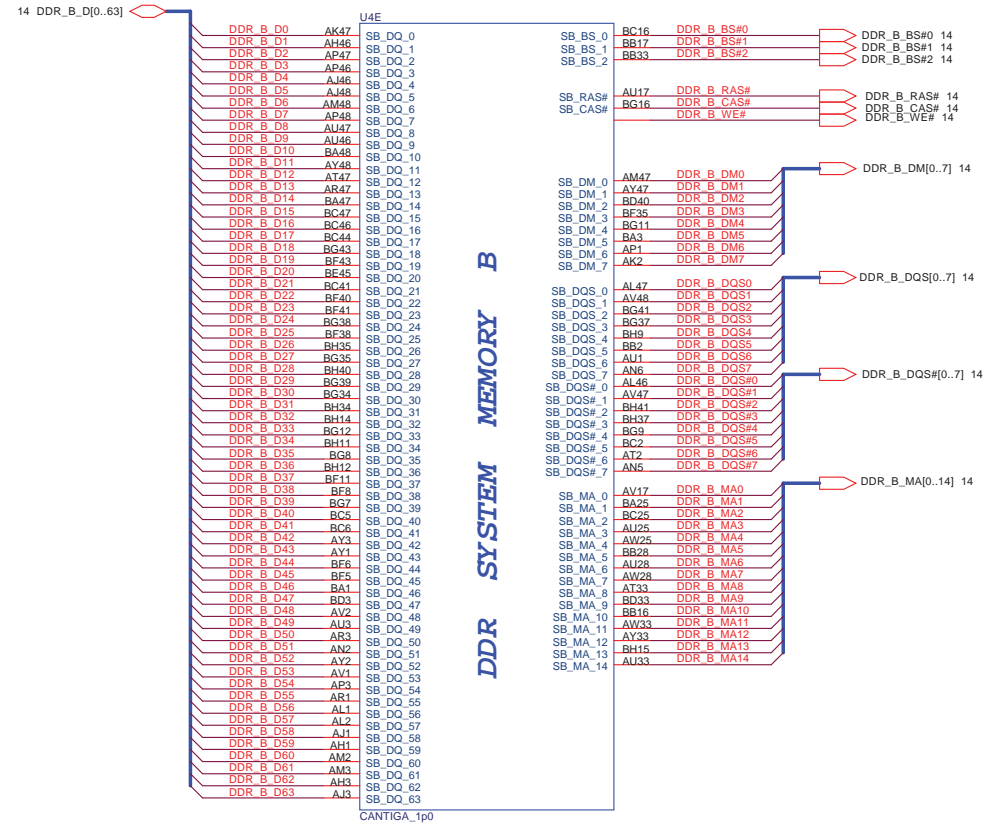
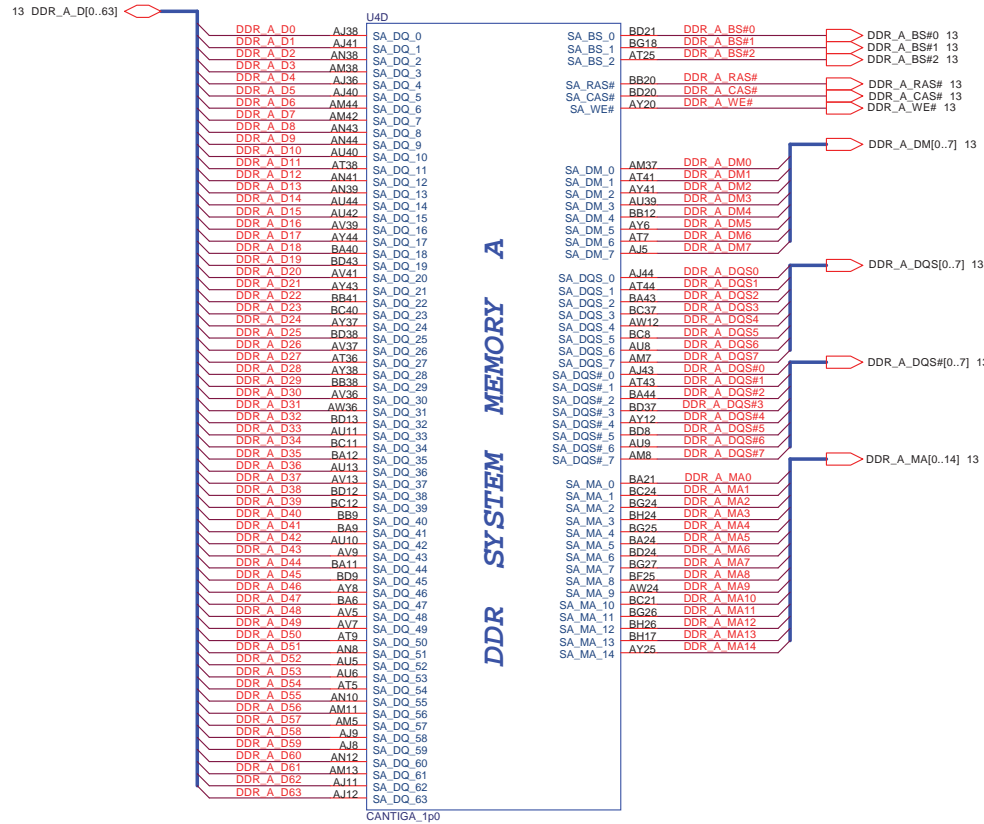
Place these inside socket cavity on L8 (North side Secondary)



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Penryn(3/3)-AGTL+/ITP-XDP			
Title	Size	Document Number	Rev
	Custom	LA-4592P	0.2
Date	Thursday, February 19, 2009	Sheet	6 of 43





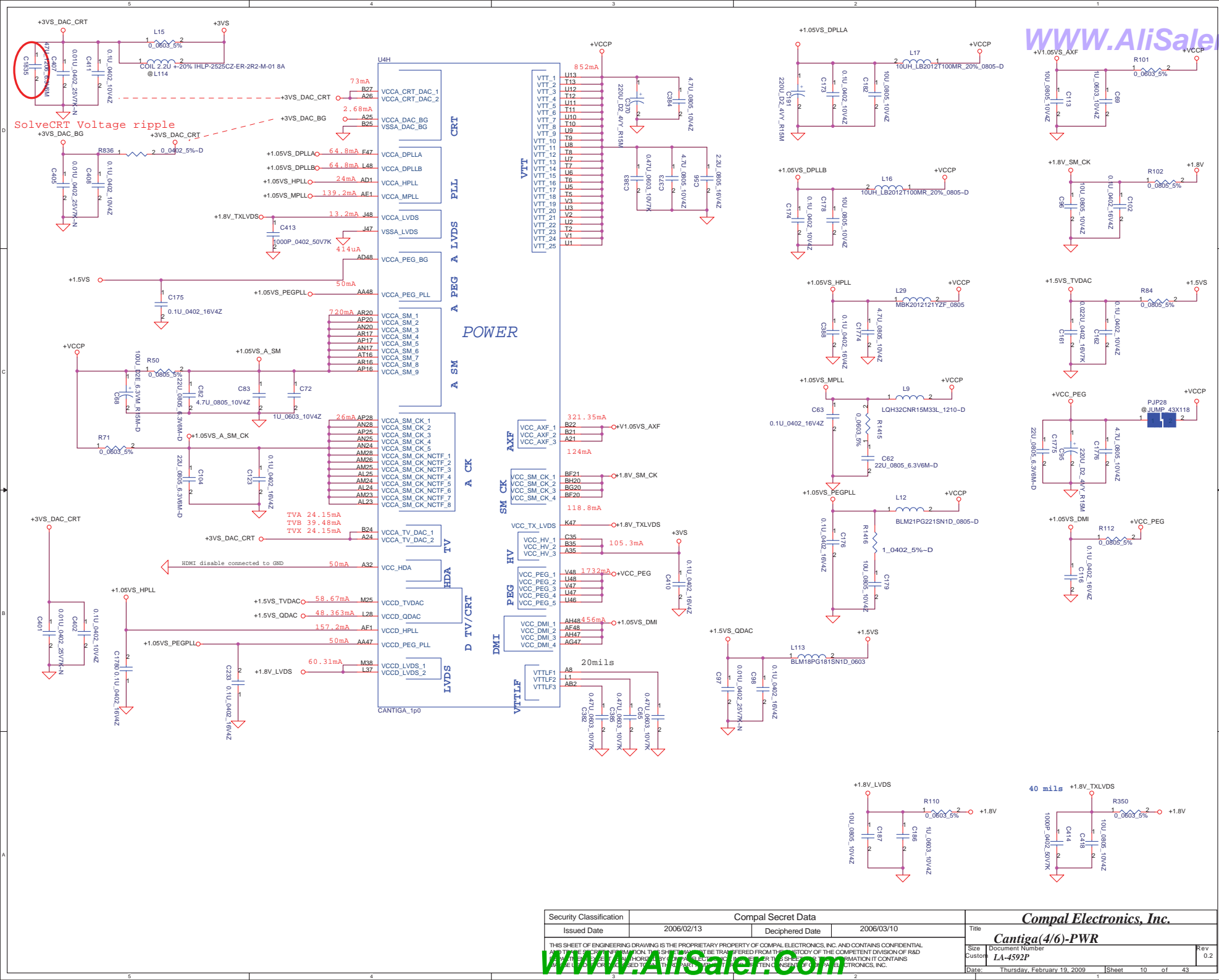
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Date: Thursday, February 19, 2009				Sheet	8 of 43



Strap Pin Table

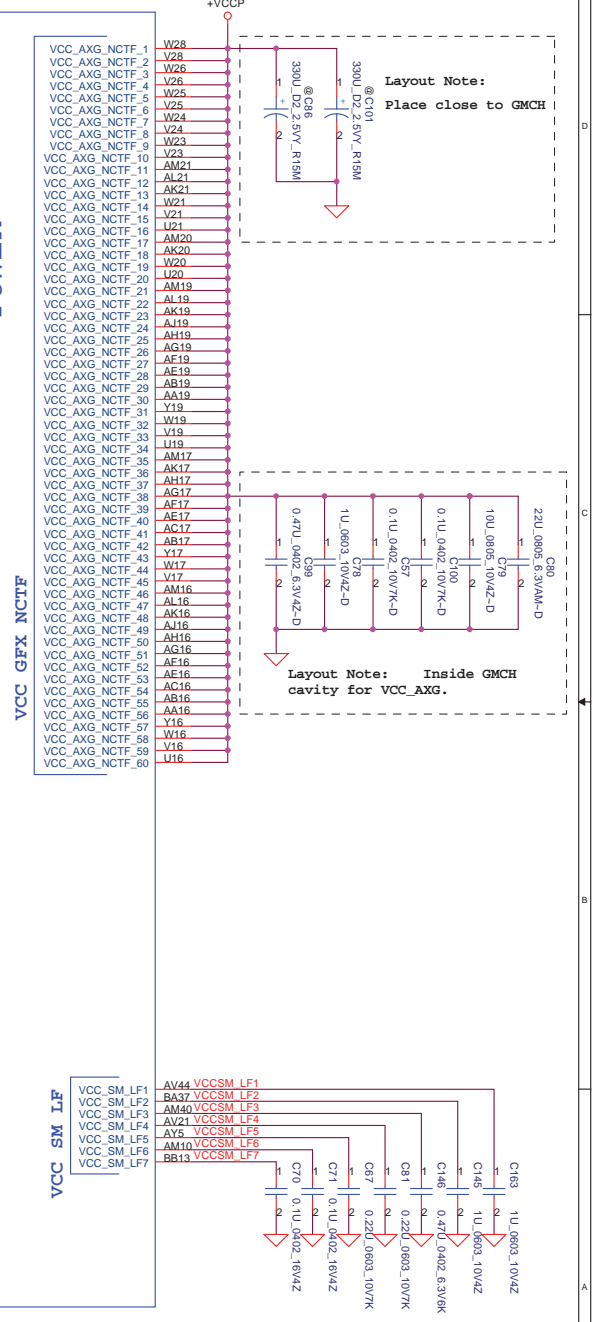
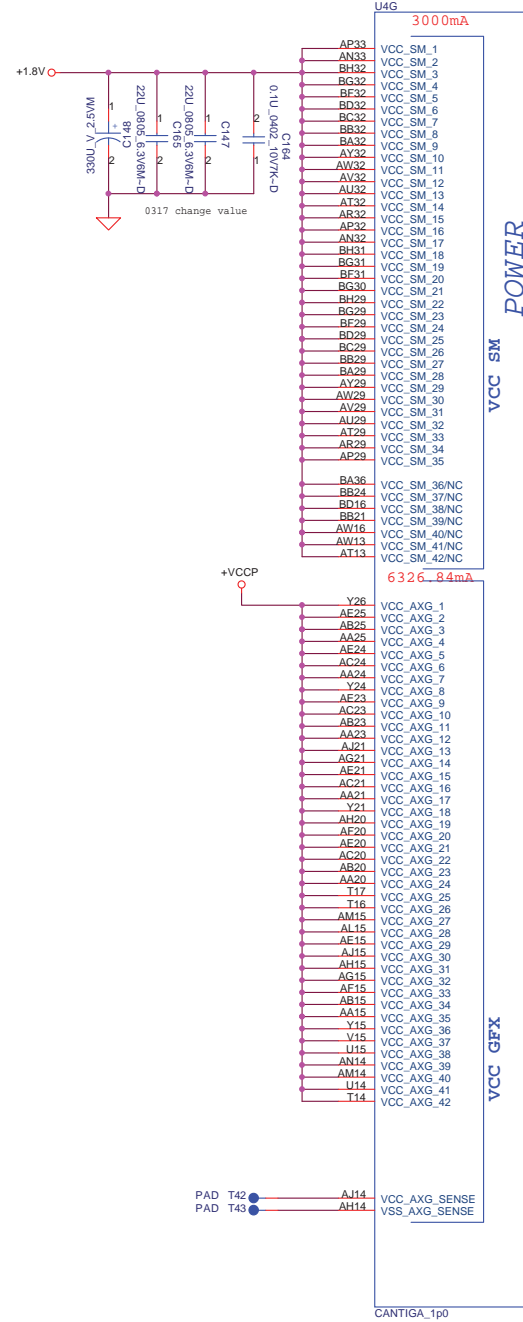
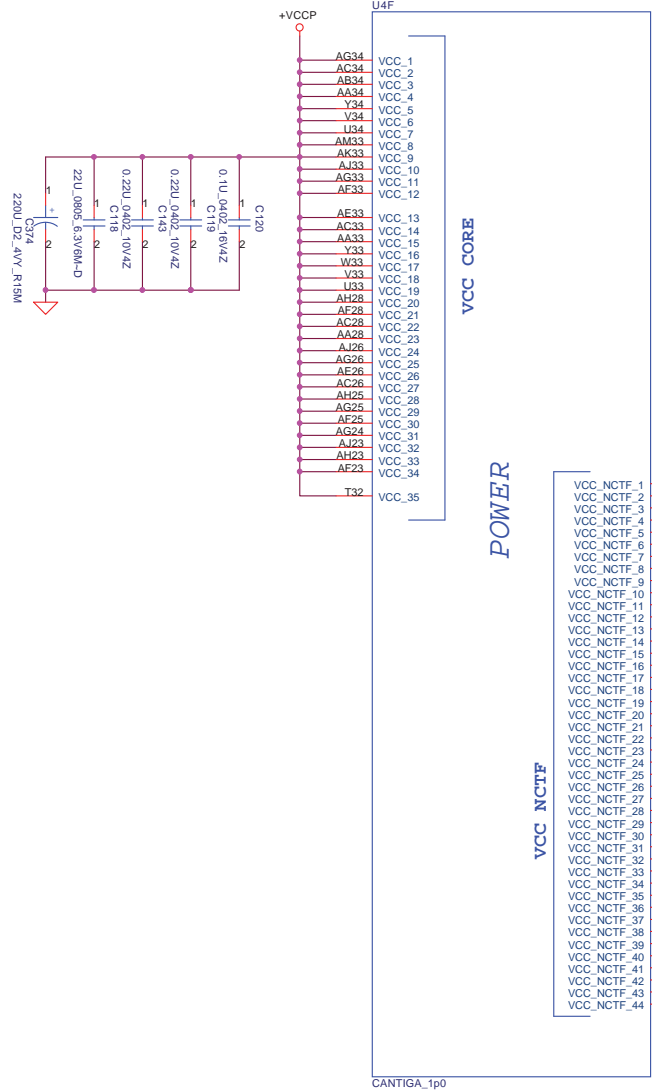


CFG[19:20] have internal pulldown



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Sheet	10	of	43		

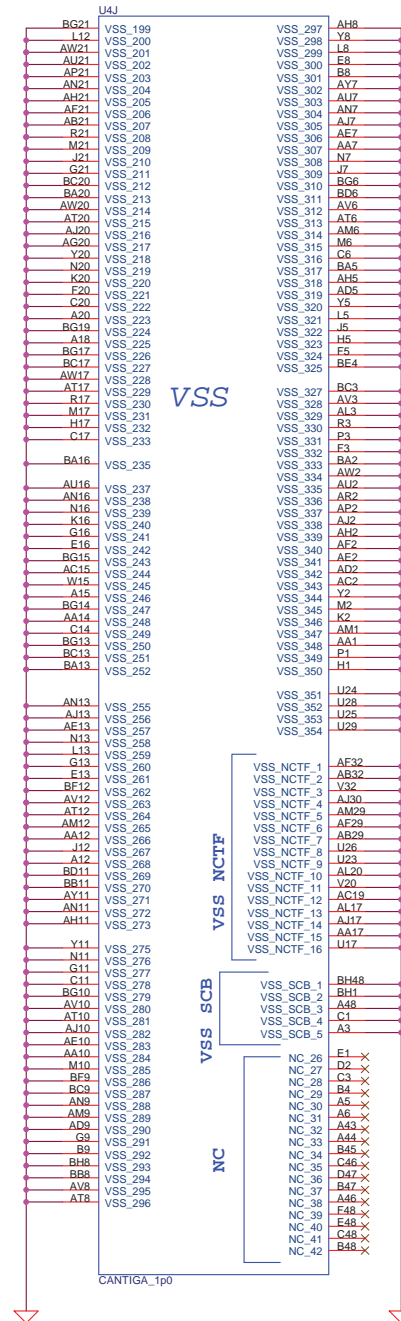
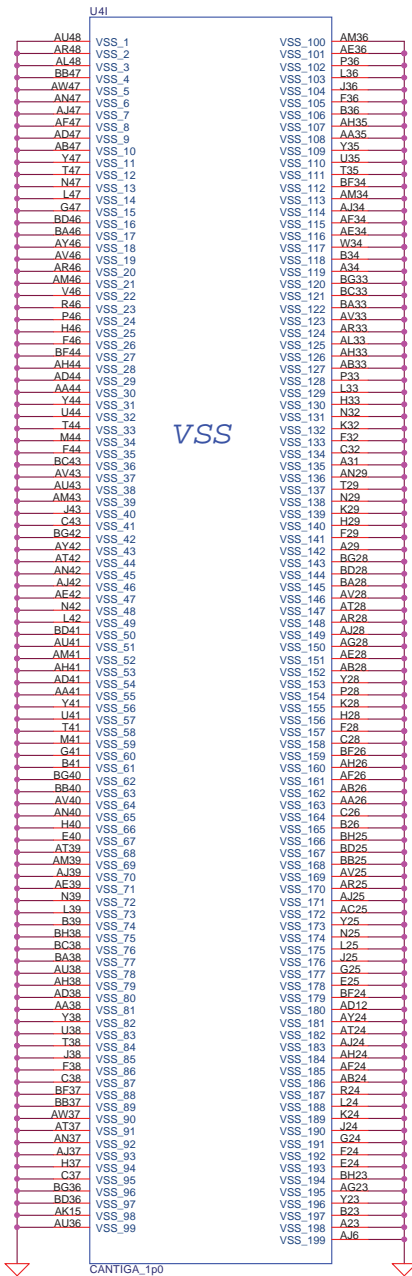
Extenal Graphic: 1210.34mA
integrated Graphic: 1930.4mA



Layout Note:
Place close to GMCH

Layout Note:
Inside GMCH cavity for VCC_AXG.

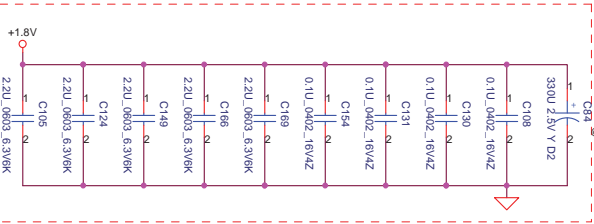
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						Customer		LA-4592P		0.2	
Date:						Thursday, February 19, 2009		Sheet 11 of 43			



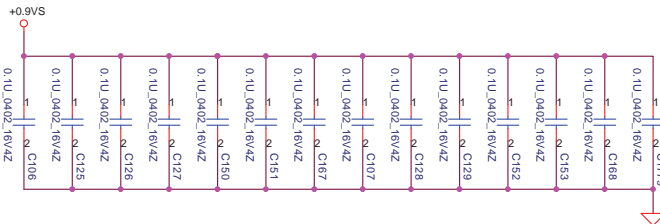
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					LA-4592P	
					Date:	Sheet
					Thursday, February 19, 2009	12 of 43



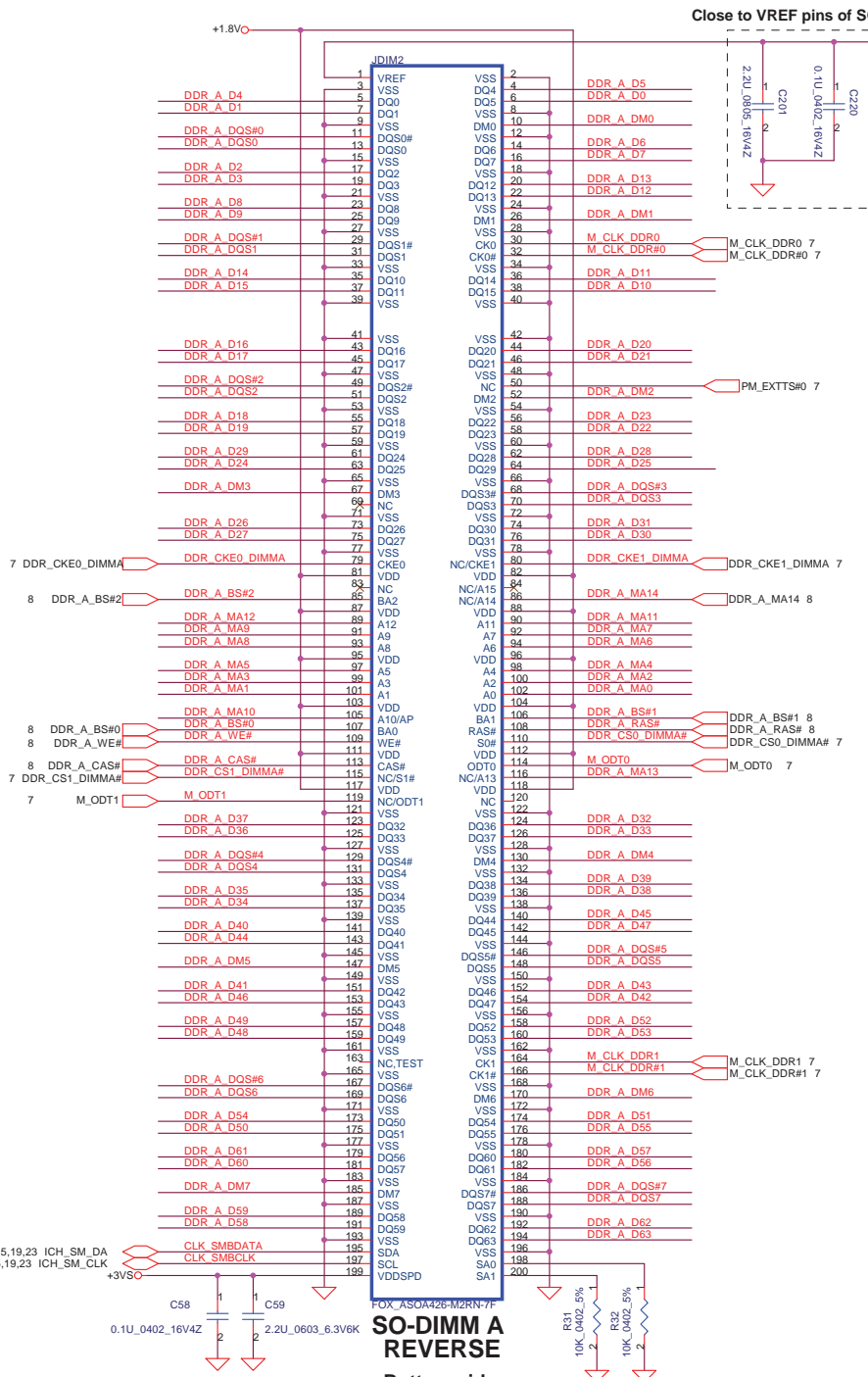
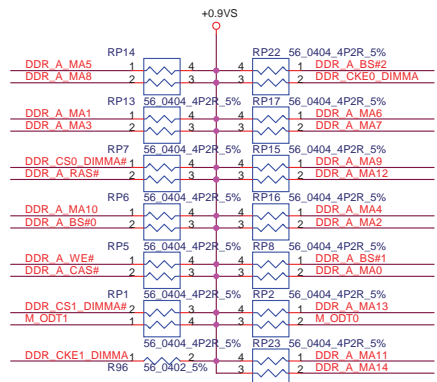
Layout Note:
Place near JDIM1



Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9V

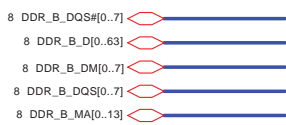


Layout Note:
Place these resistor closely JP41, all trace length Max=1.5"

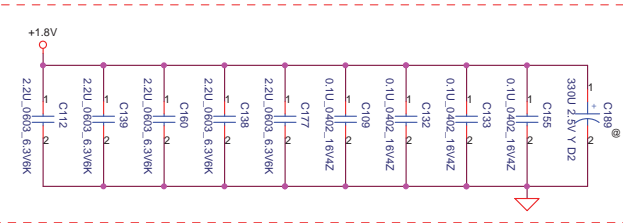


SO-DIMM A
REVERSE
Bottom side

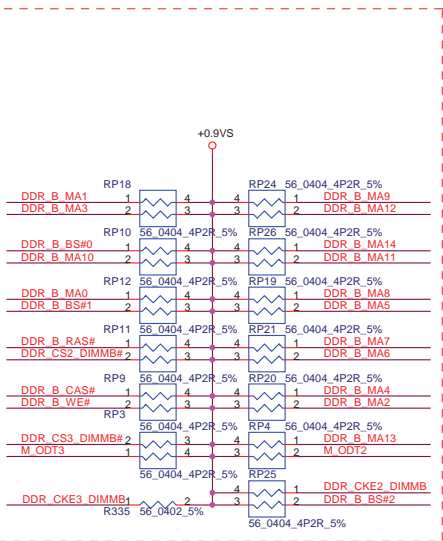
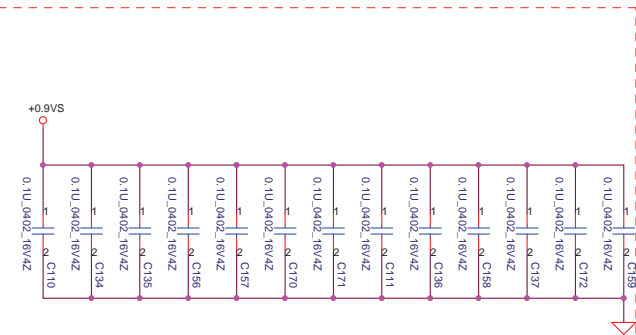
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				DDR2 SO-DIMM 1					
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				LA-4592P				0.2	
				Date:		Thursday, February 19, 2009		Sheet 13 of 43	



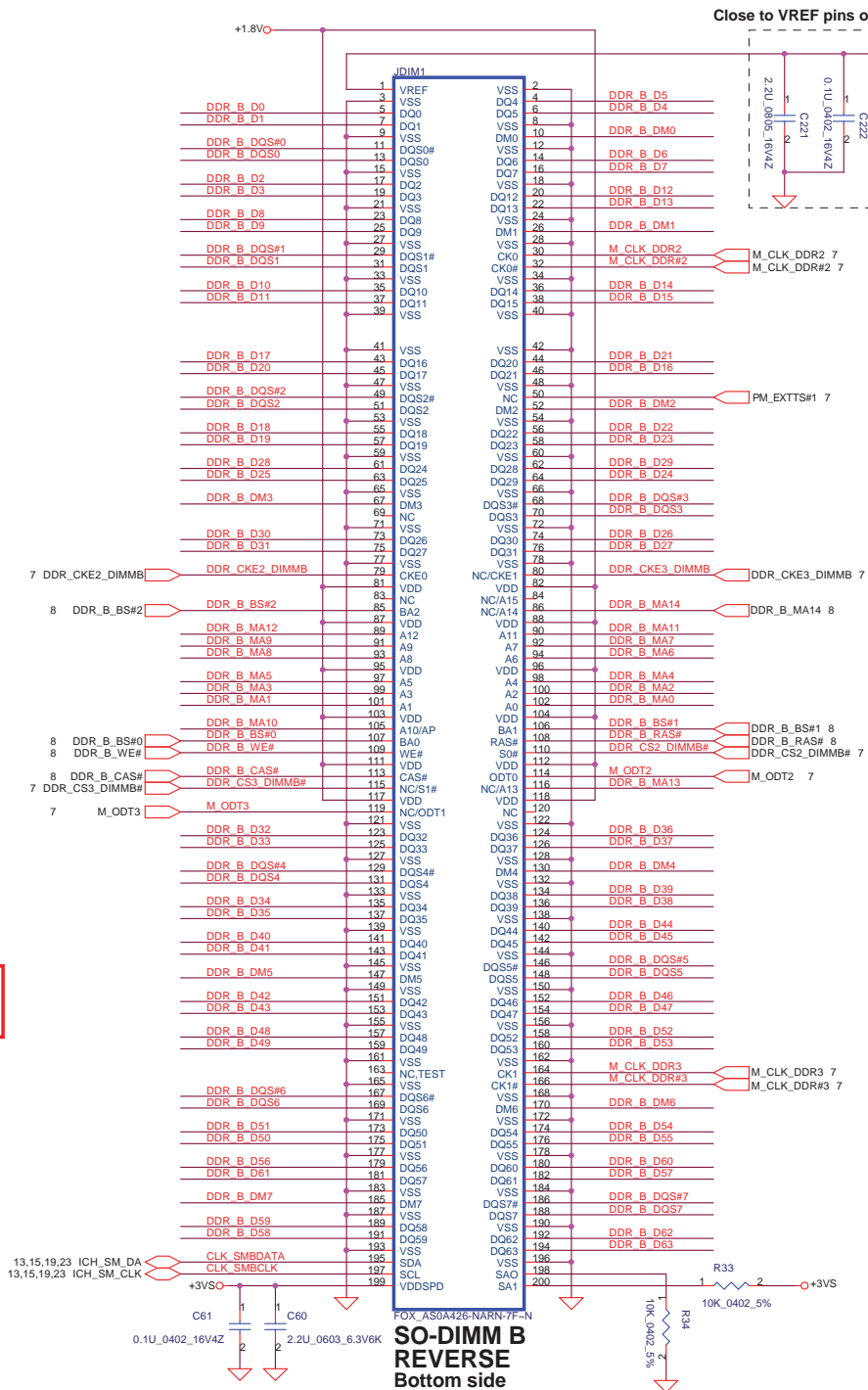
Layout Note:
Place near JDIM2



Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9VS

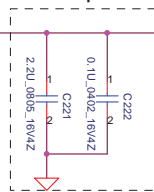


Layout Note:
Place these resistor closely JP42, all trace length Max=1.5"



SO-DIMM B
REVERSE
Bottom side

Close to VREF pins of SO-DIMM

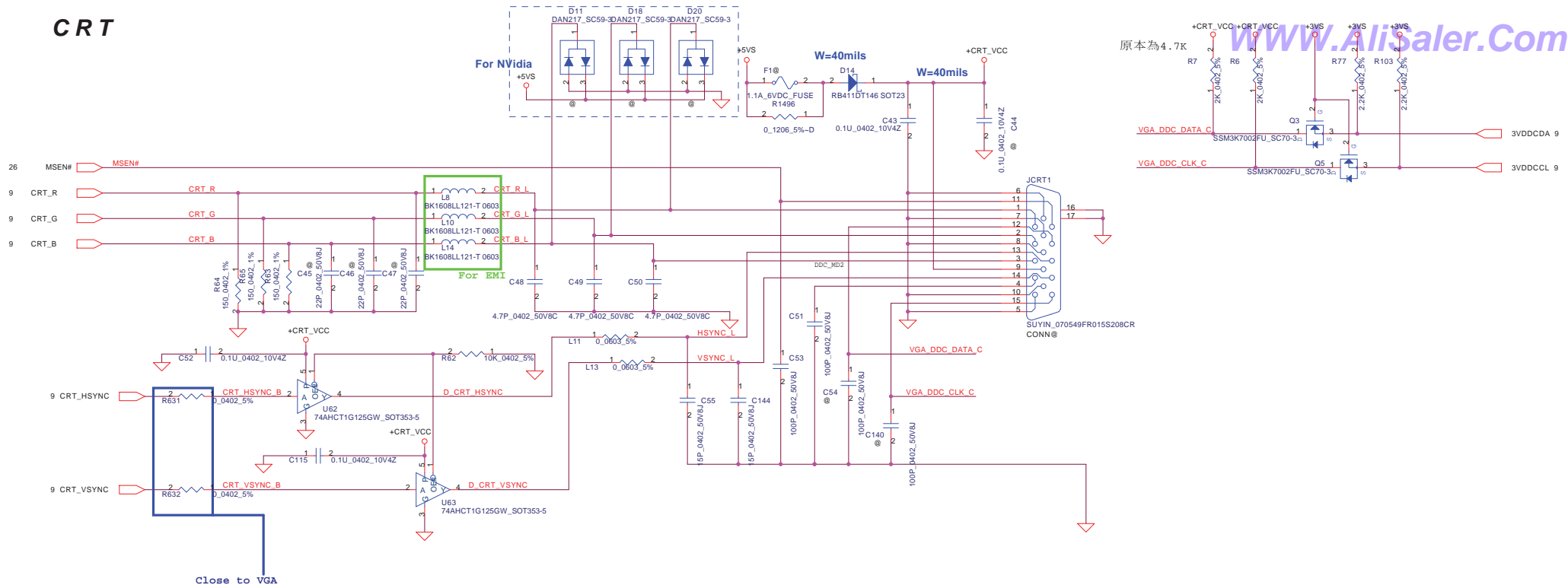


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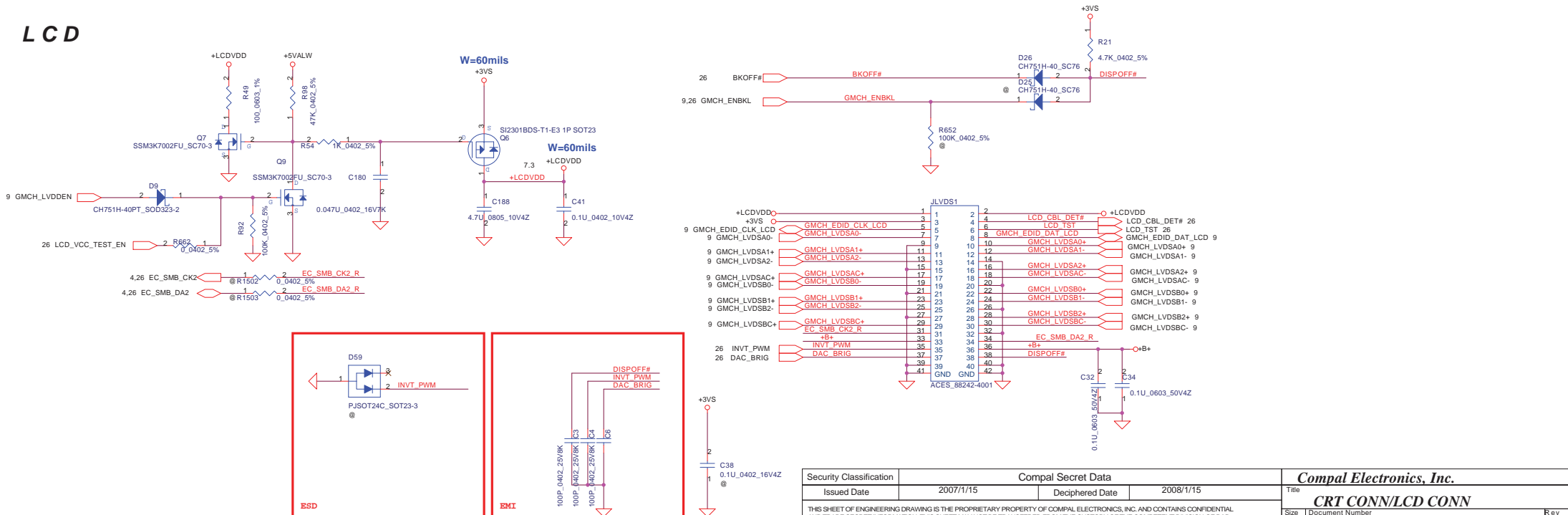
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				Date:	Thursday, February 19, 2009	Sheet 14 of 43

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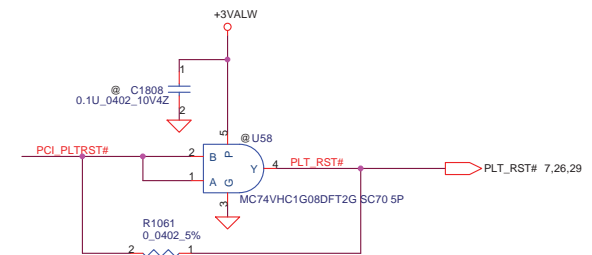
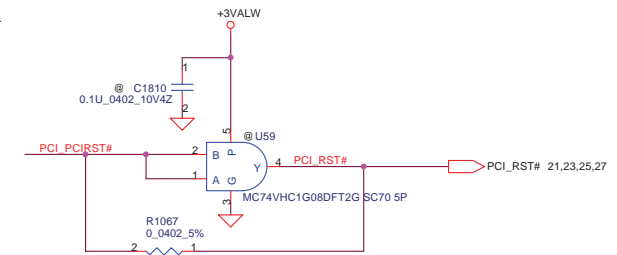
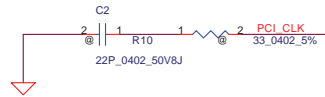
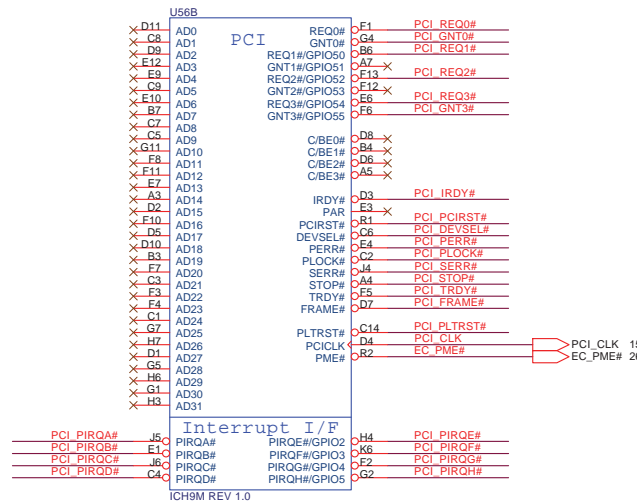
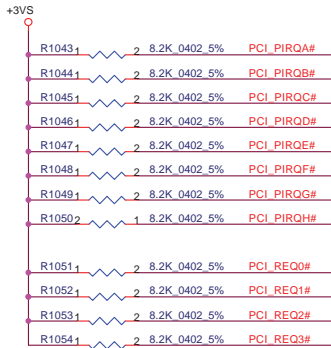
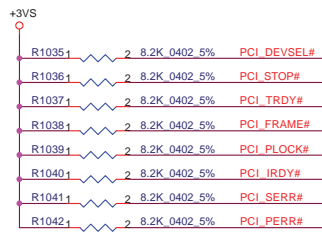
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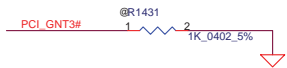
LCD



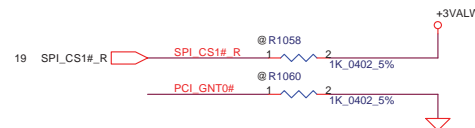
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Size	Document Number				
Custom	LA-4592P				
Date:	Thursday, February 19, 2009	Sheet	16	of	43



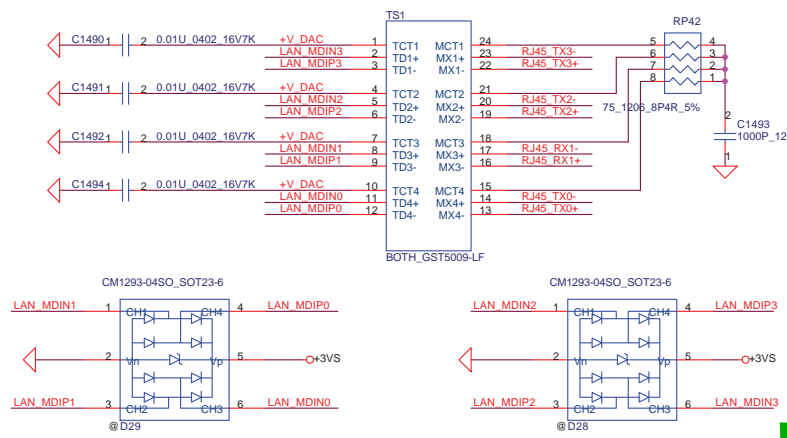
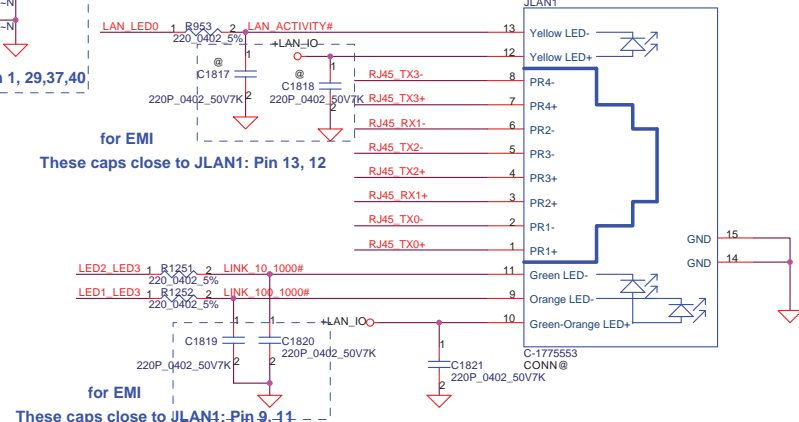
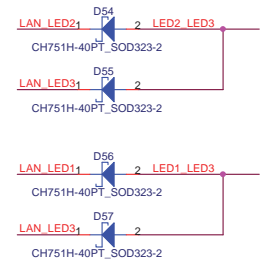
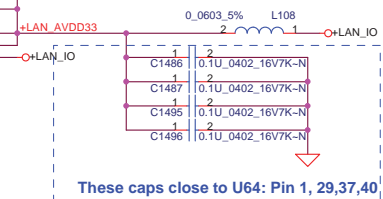
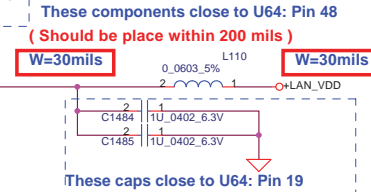
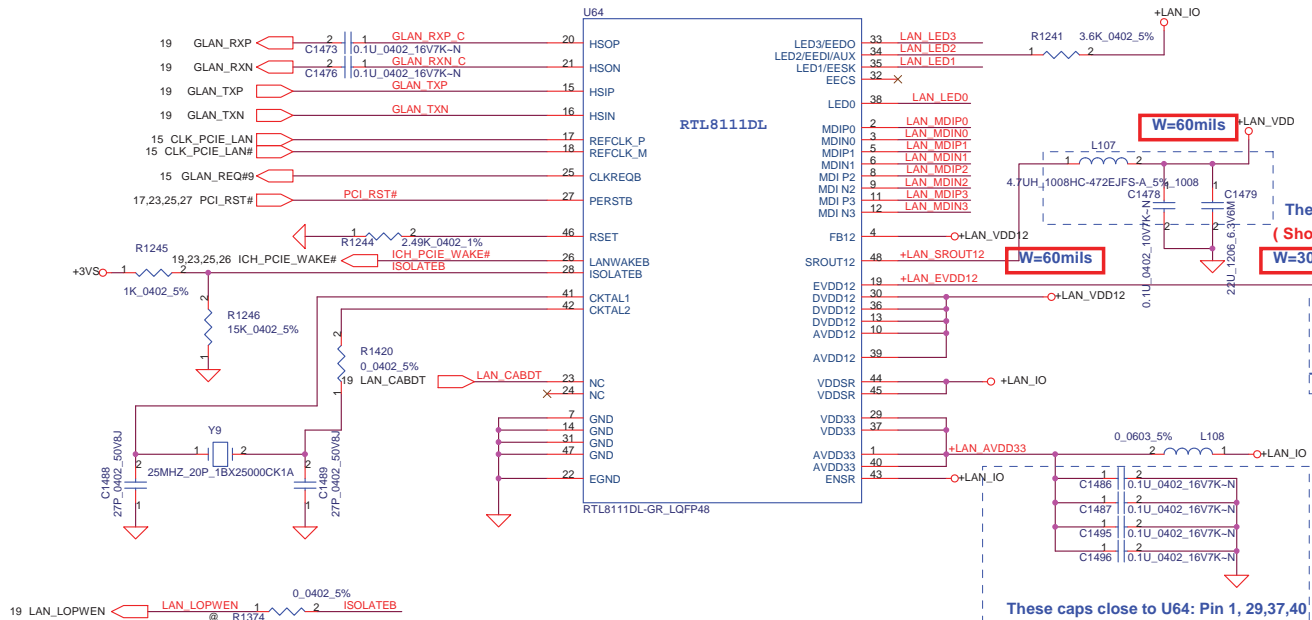
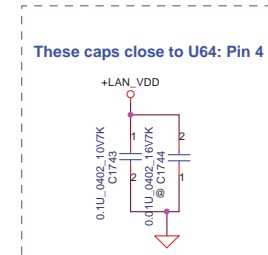
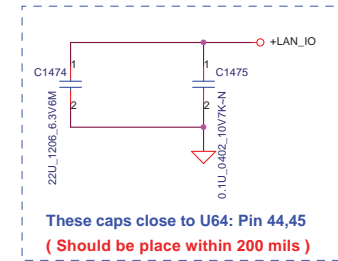
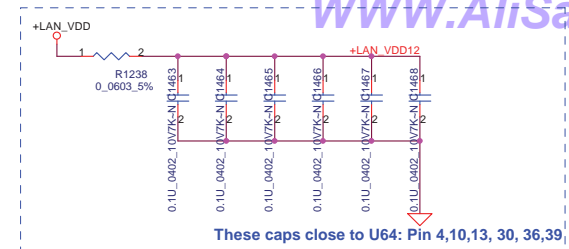
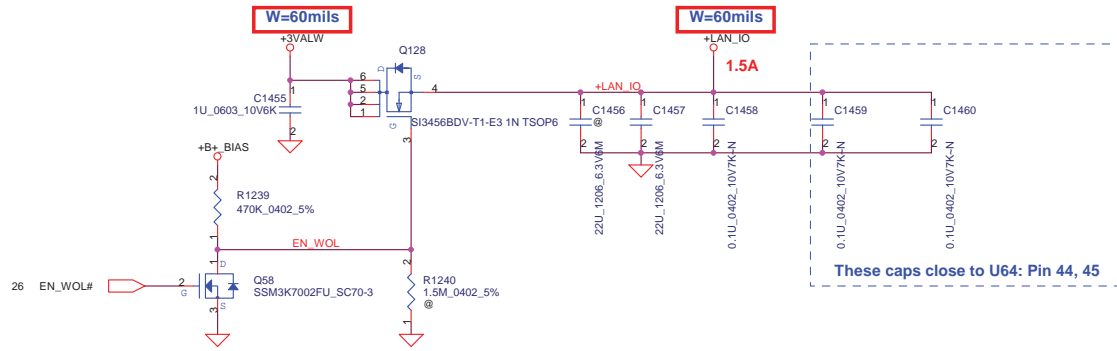
A16 swap override Strap	
PCI_GNT3#	Low= A16 swap override Enable High= Default *



Boot BIOS Strap		
PCI_GNT0#	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC *

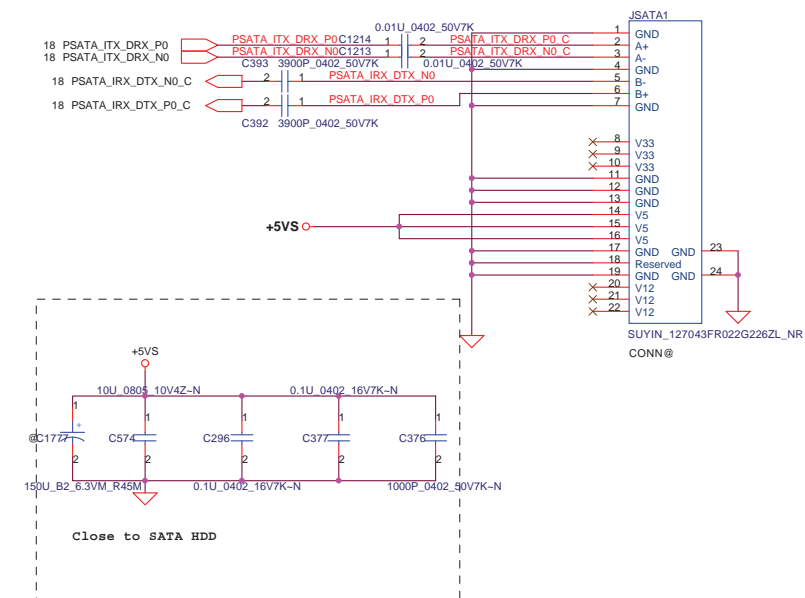




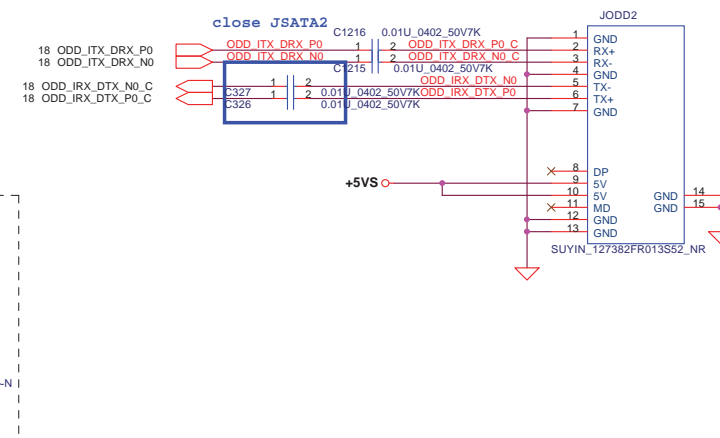


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				Custody	LA-4392P	0.2	
				Date:	Thursday, February 19, 2009	Sheet	21 of 43

SATA HDD CONN

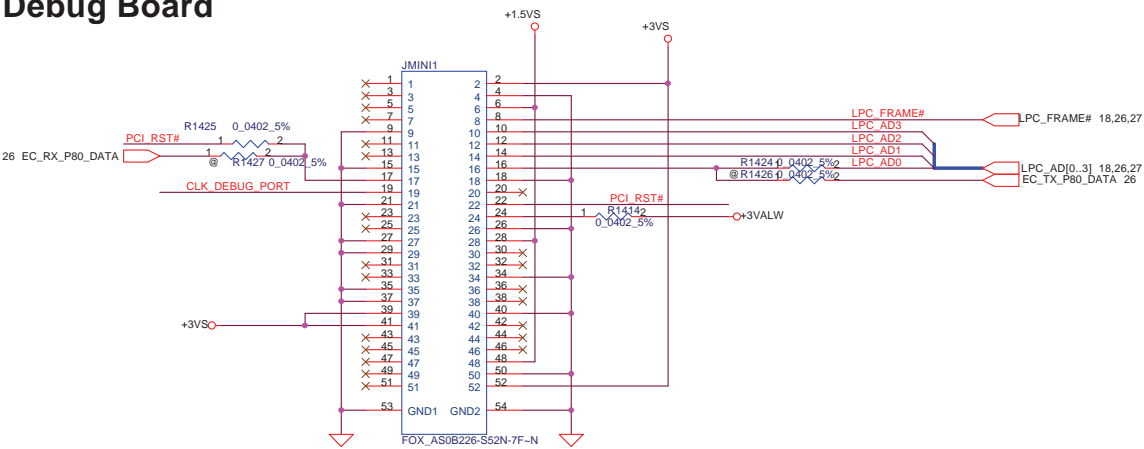


SATA ODD CONN

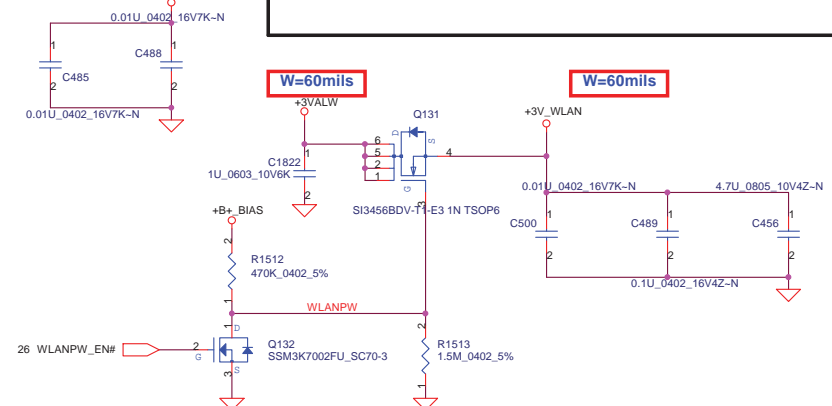
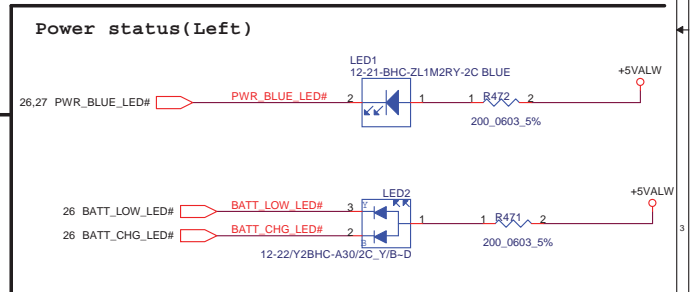
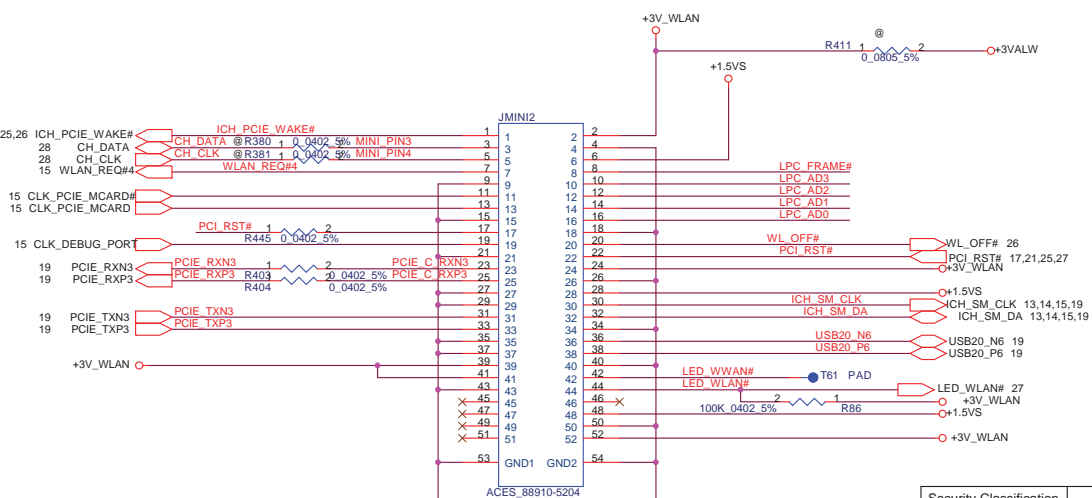


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				Customer	LA-4592P
				Date	Thursday, February 19, 2009
				Sheet	22 of 43
				Rev	0.2

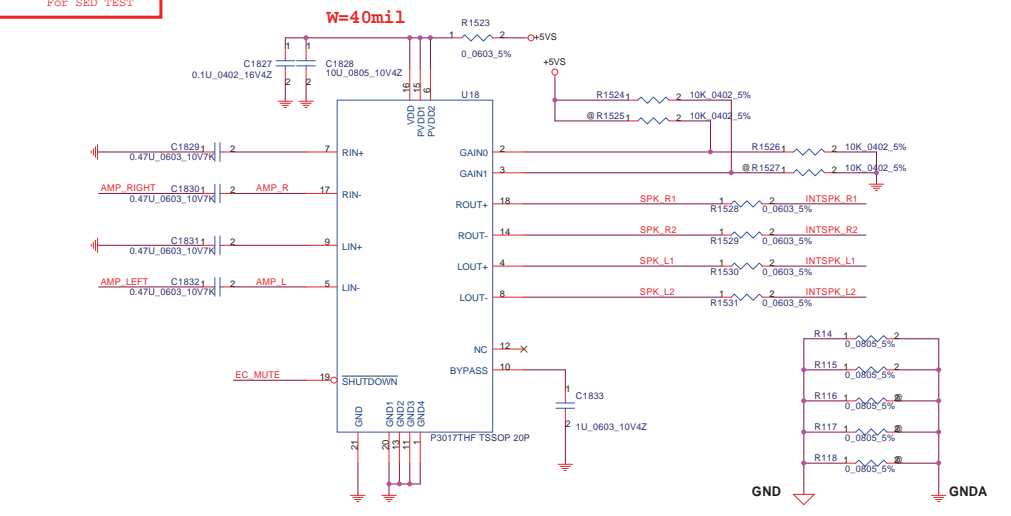
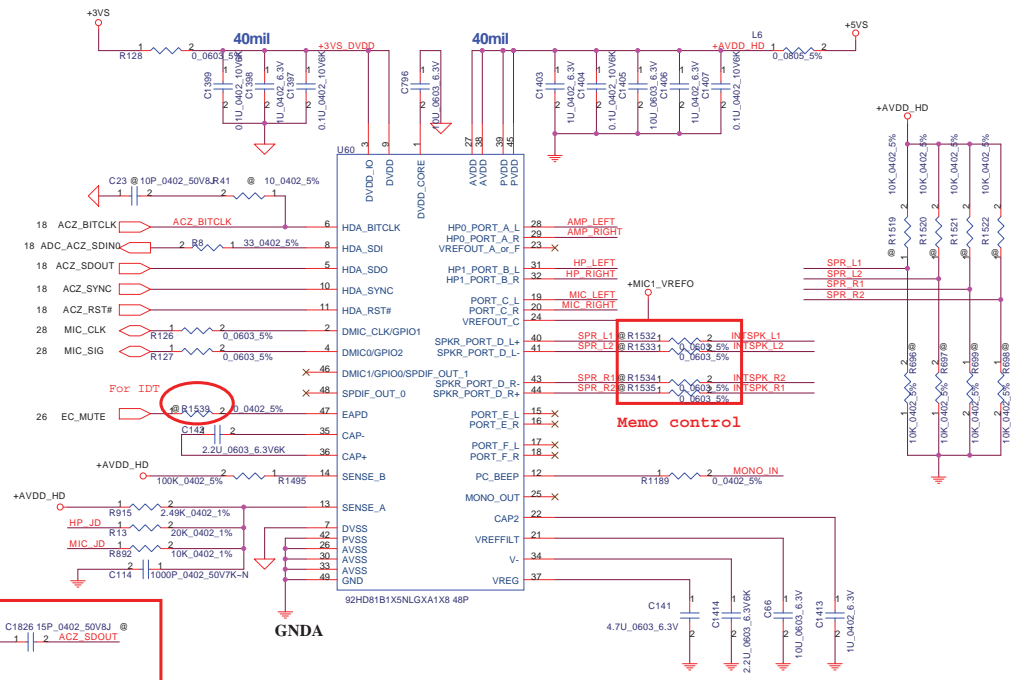
Debug Board



Mini-Express Card---WLAN

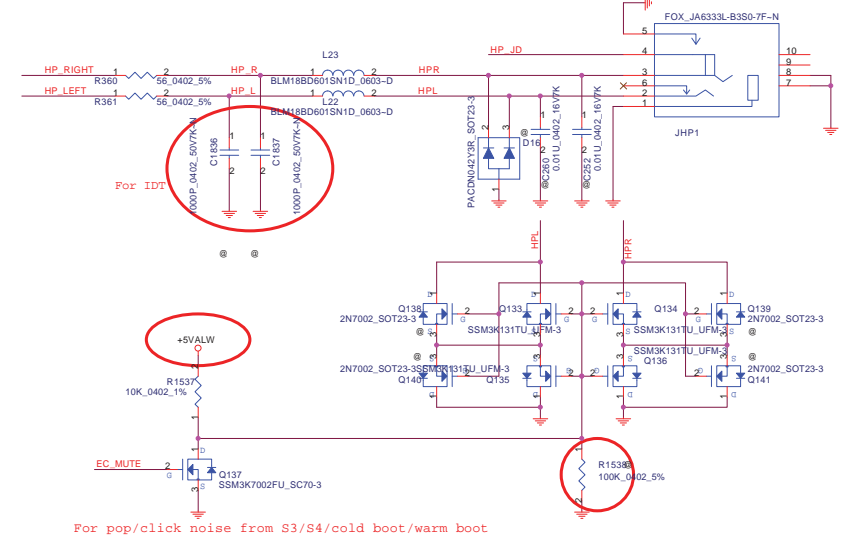


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				Size Custom	Document Number LA-4592P	Rev 0.2
				Date: Thursday, February 19, 2009		Sheet 23 of 43

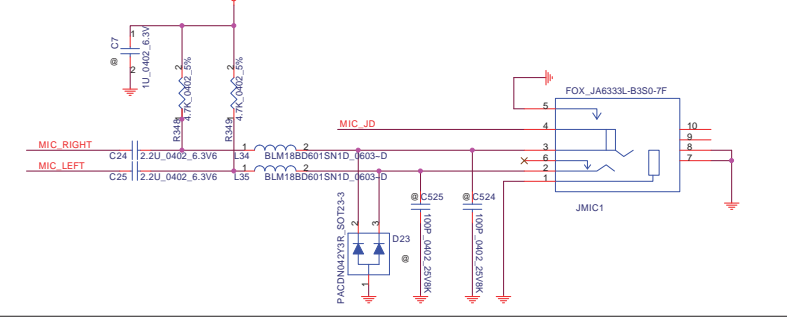


GAIN0	GAIN1	GAIN
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB

HEADPHONE OUT JACK



MICROPHONE IN JACK



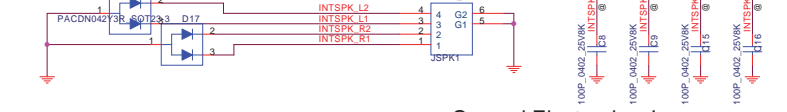
EC Beep



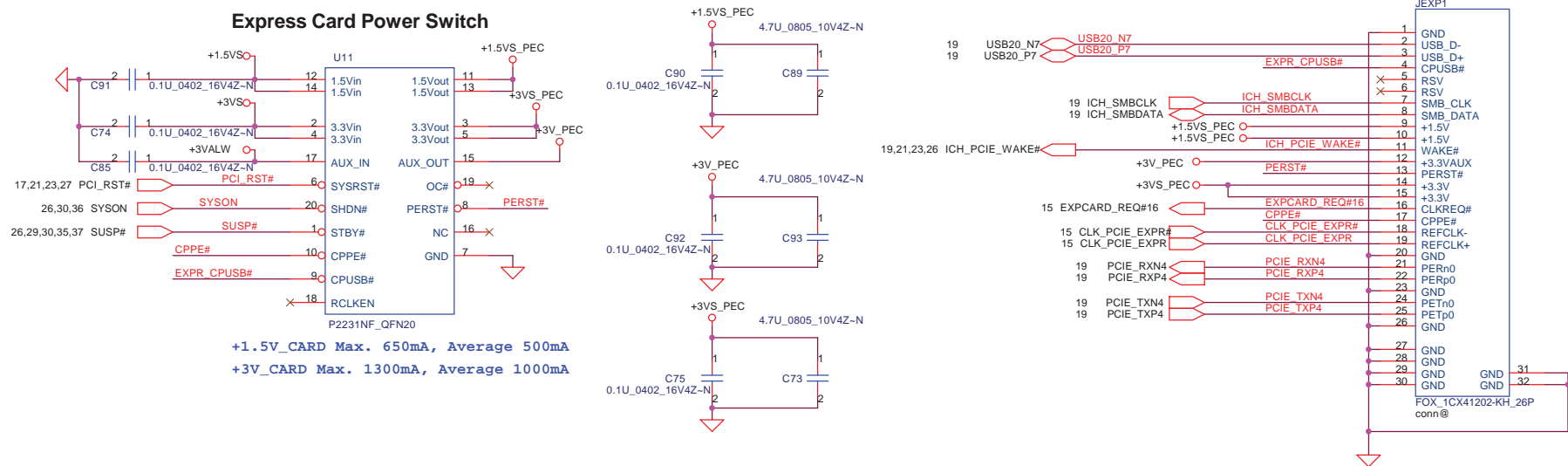
ICH Beep



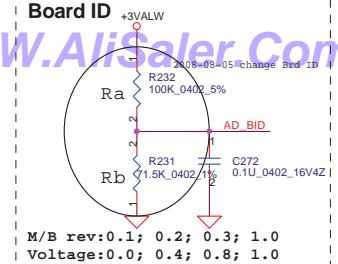
Speaker Connector



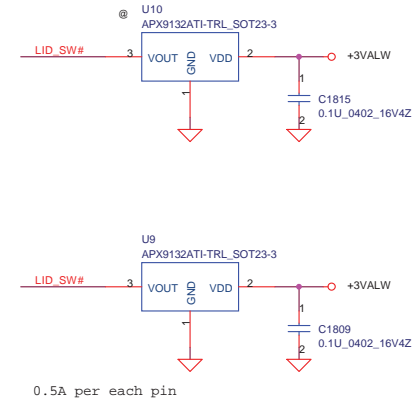
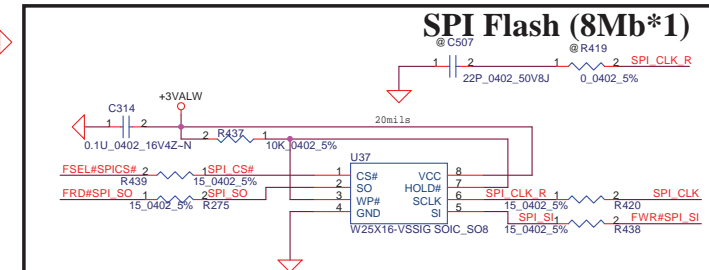
Compal Electronics, Inc.



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Issued Date	2007/1/15	Deciphered Date	2008/1/15	Title	EXPRESS CARD
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				Date: Thursday, February 19, 2009	Rev 0.2
				Sheet 25 of 43	



VCC	3.3V/5V	0.6V-1.8V
No	10K	
Board ID	0	0.000
0	26.1K +/-1%	0.000
1	46.8K +/-1%	0.000
2	46.8K +/-1%	0.000
3	46.8K +/-1%	0.000
4	46.8K +/-1%	0.000
5	46.8K +/-1%	0.000



0.5A per each pin

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Size	Document Number	Rev		
Custom	LA-4592P	0.2		
Date:	Thursday, February 19, 2009	Sheet	26	of 43

80 mils

80 mils

80 mils

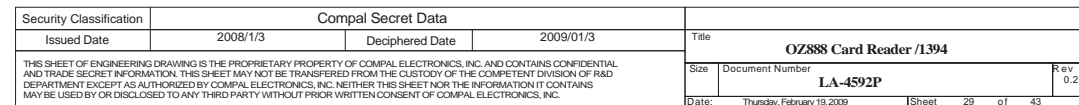
Check Module pin define Camera Conn

Fingerprint

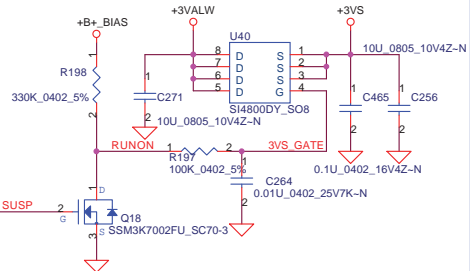
Bluetooth

Felica Conn

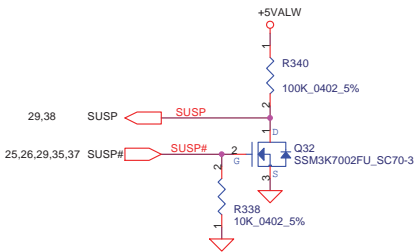
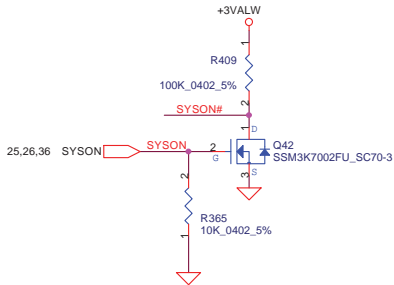
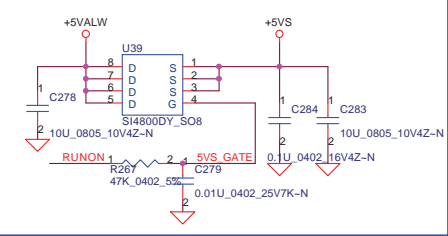
Security Classification				Compal Secret Data				Compal Electronics, Inc.			
Issued Date		2007/1/15		Deciphered Date		2008/1/15		Title			
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Size		Document Number		Custom		Rev		0.2			
Date:		Thursday, February 19, 2009		Sheet		28		of 43			



+3VALW to +3VS Transfer

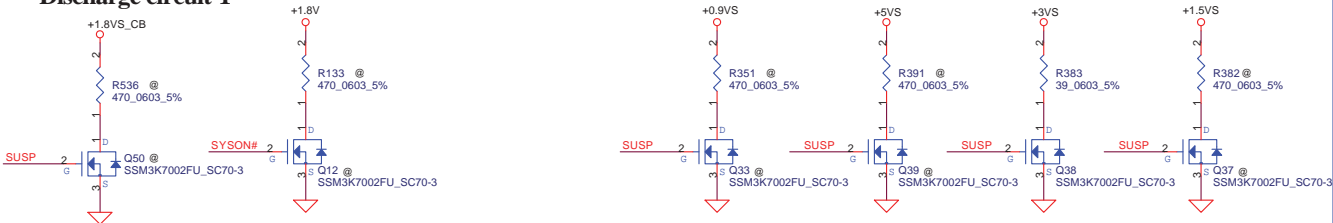


+5VALW to +5VS Transfer

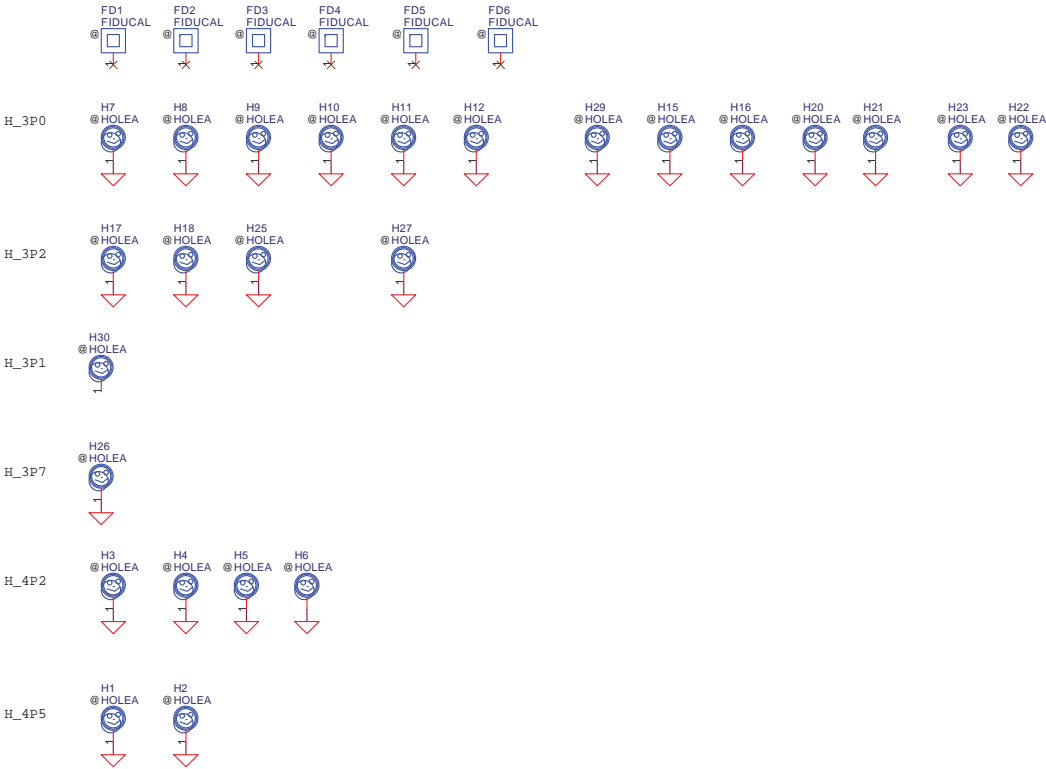


VGA Discharge circuit

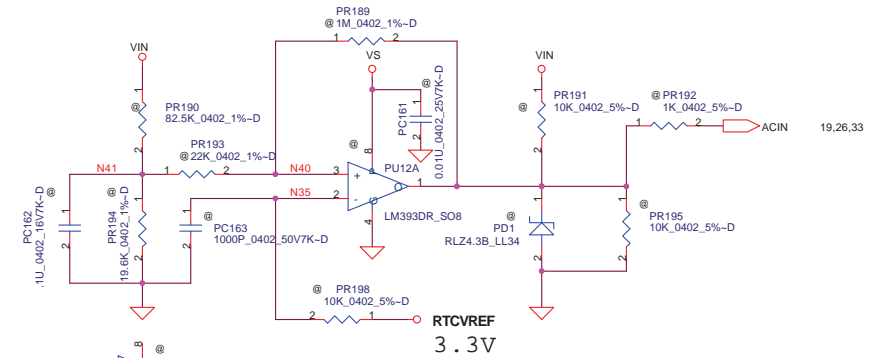
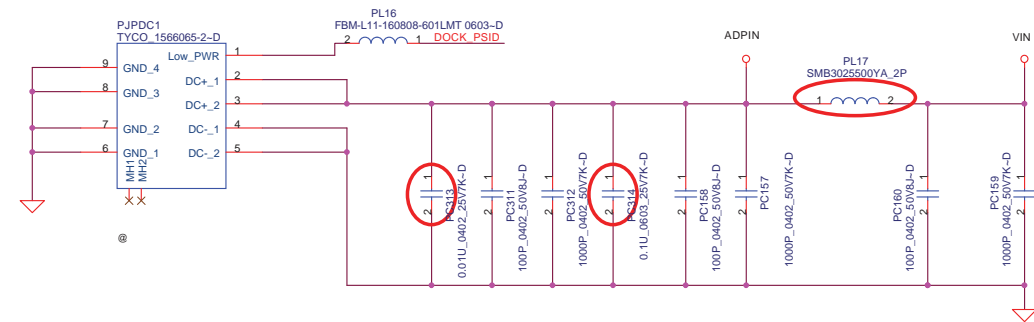
Discharge circuit-1



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Date: Thursday, February 19, 2009				Size	Document Number
Sheet 30 of 43				Custom	LA-4592P
				Rev	0.2

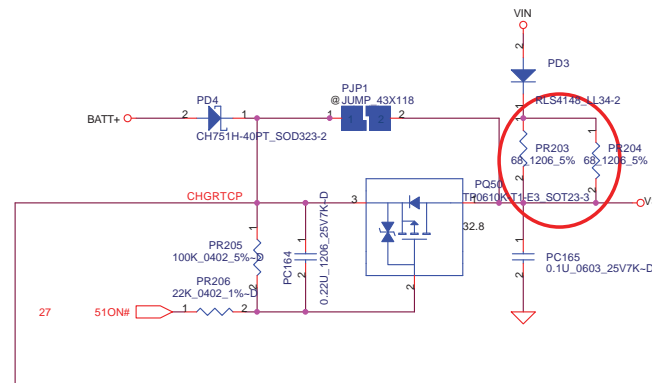


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				Size Custom	Document Number LA-4592P Rev 0.2
				Date: Thursday, February 19, 2009	Sheet 31 of 43

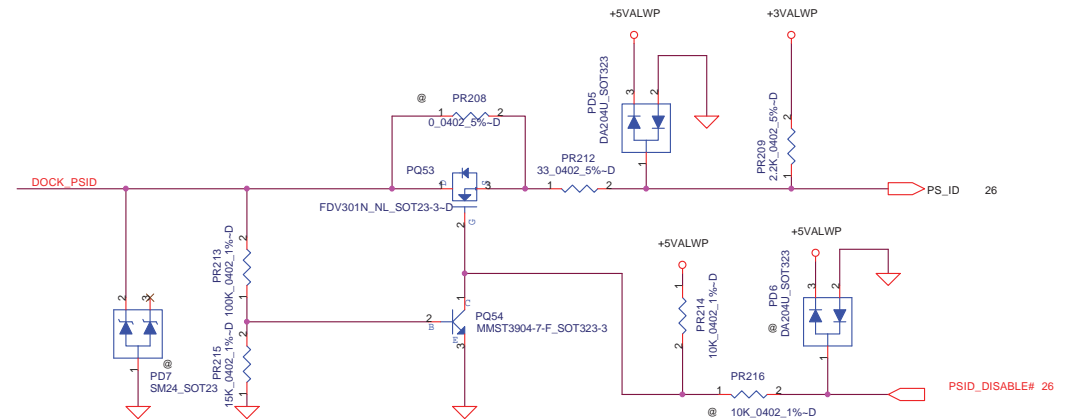
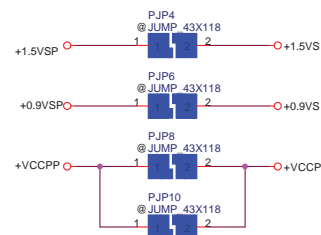
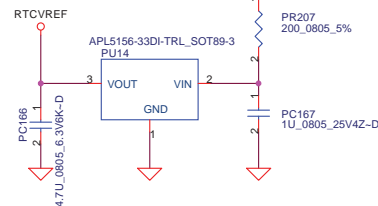


Vin Detector

	Max.	typ.	Min.
L-->H	18.234	17.841	17.449
H-->L	17.597	17.210	16.813

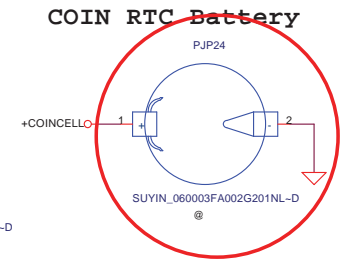
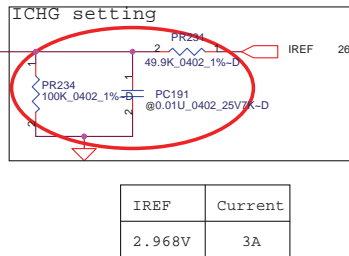
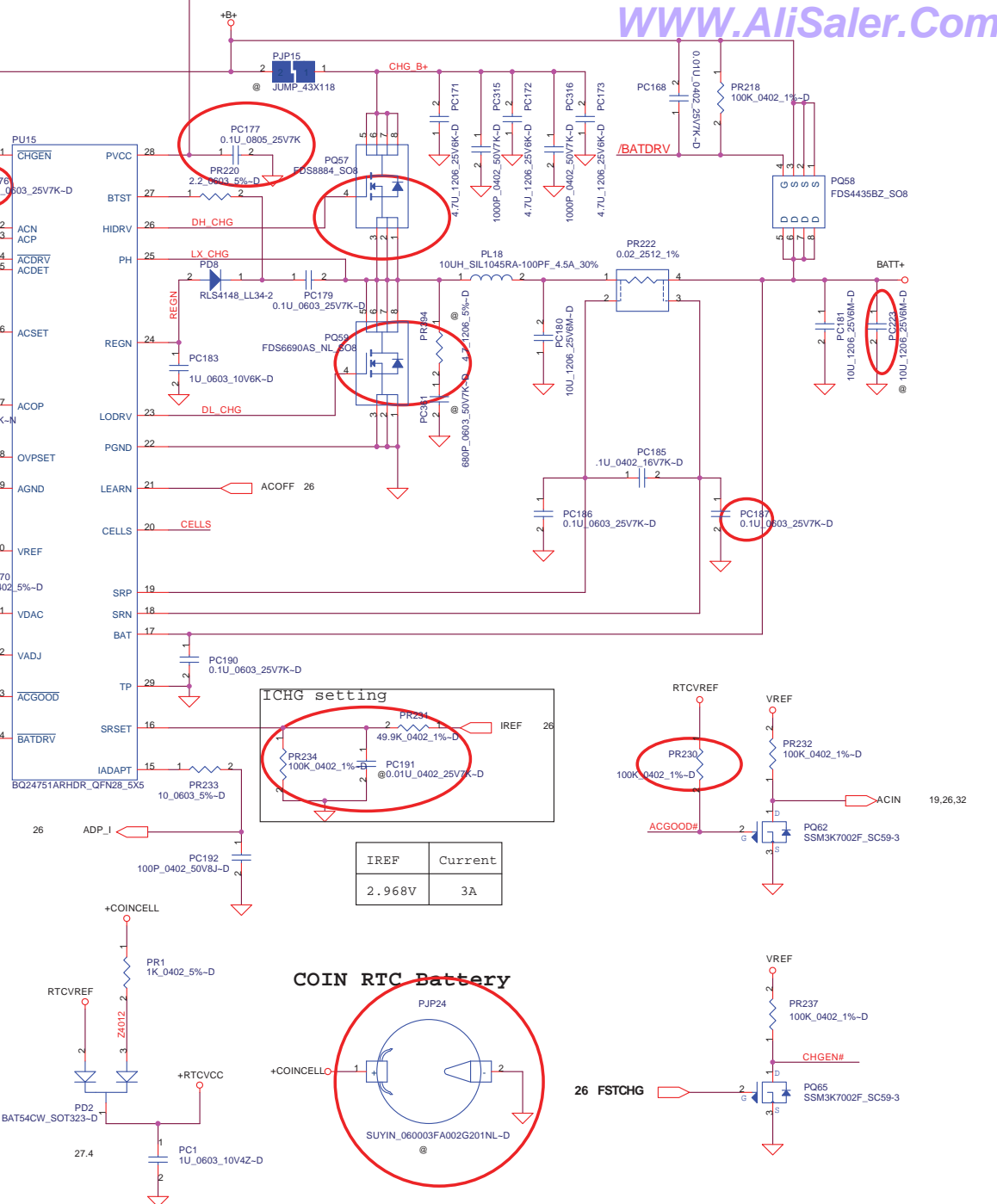
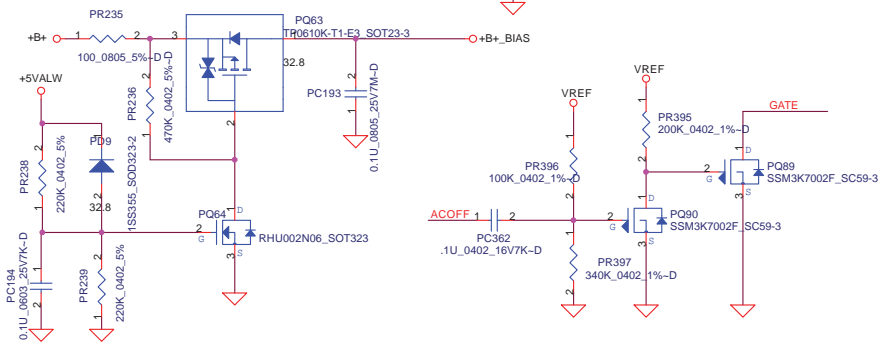
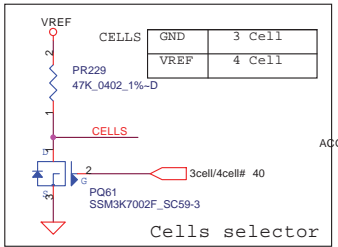


3.3V

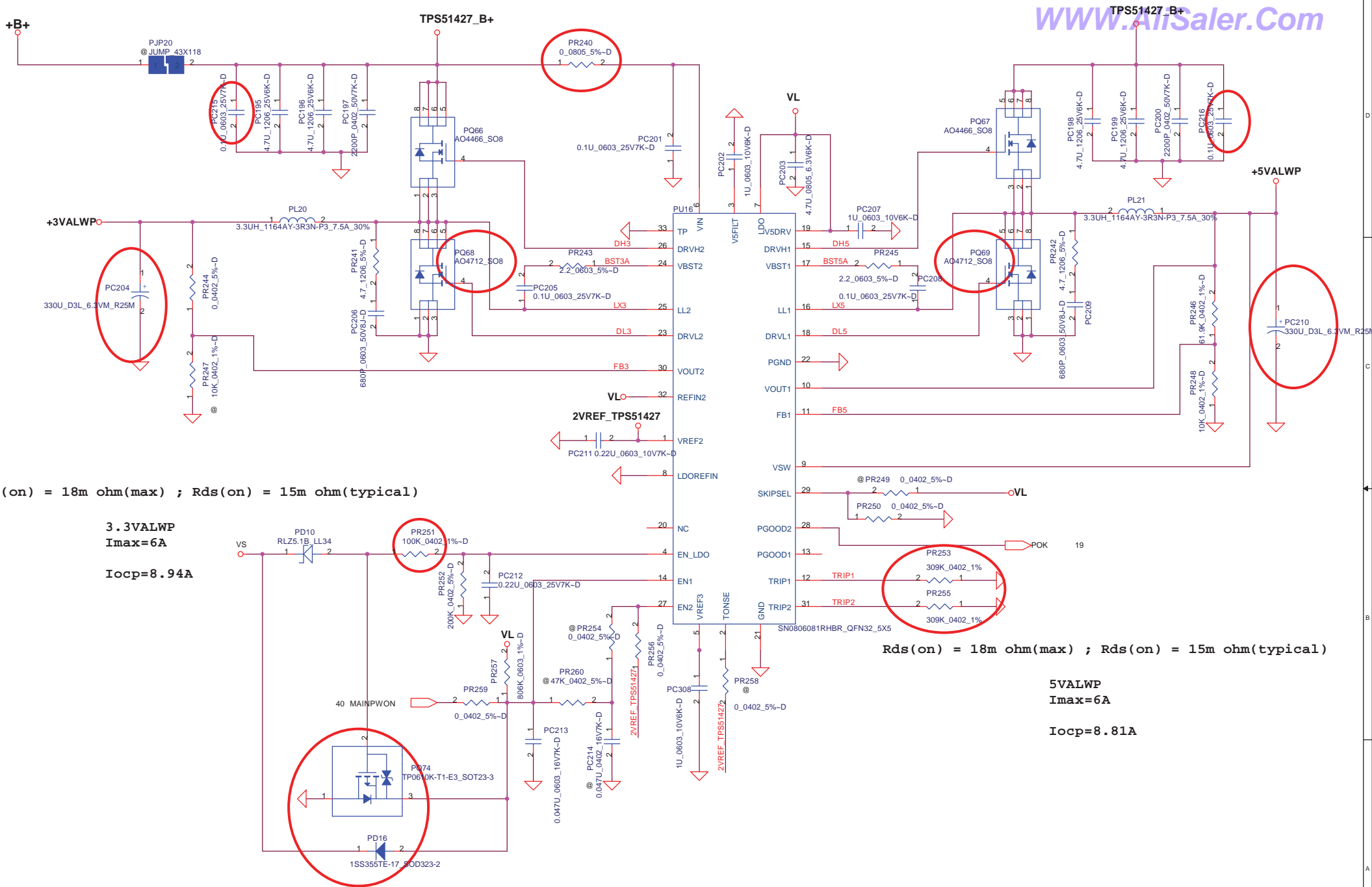


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				Size	Document Number	Rev	
Custom		LA-4596P		0.2			
Date:		Thursday, February 19, 2009		Sheet	32	of 43	

90W adapter
 $I_{charge} = (V_{srset}/V_{vdac}) * (0.1/PR34) = 3.34A$
 $I_{adapter} = (V_{acset}/V_{vdac}) * (0.1/PR17) = 3.1A$
 Input OVP : 22.3V
 Input UVP : 16.98V
 Fsw : 300KHz



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Size	B	Document Number	KML50	Rev	0.2
Date	Thursday, February 19, 2009	Sheet	33	of	43



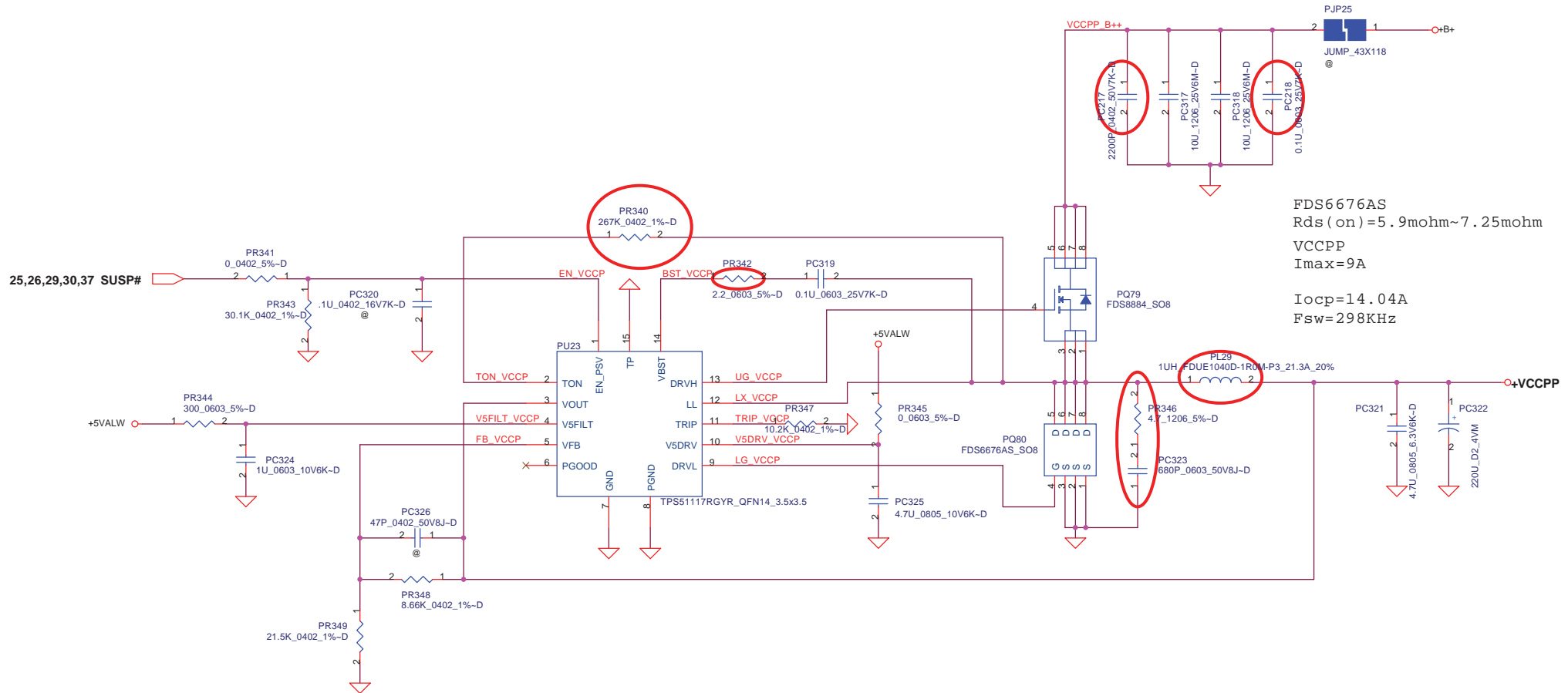
Rds(on) = 18m ohm(max) ; Rds(on) = 15m ohm(typical)

3.3VALWP
Imax=6A
Iocp=8.94A

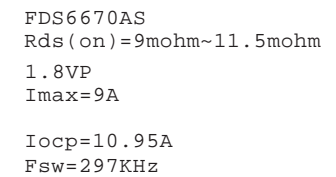
Rds(on) = 18m ohm(max) ; Rds(on) = 15m ohm(typical)

5VALWP
Imax=6A
Iocp=8.81A

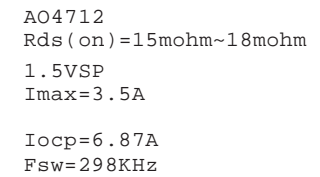
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Issued Date	2006/10/1	Deciphered Date	2007/05/30	Title	
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Size	Custom	Document Number	LA-4596P	Rev	
Date:	Thursday, February 19, 2009	Sheet	34 of 43	0.2	



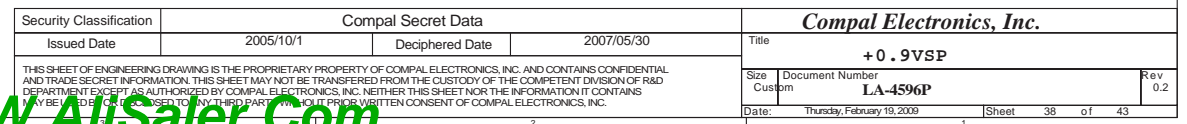
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Issued Date	2008/2/5	Deciphered Date	2009/2/5	Title	
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				LA-4596P	
				Rev	0.1
				Date:	Thursday, February 19, 2009
				Sheet	35 of 43

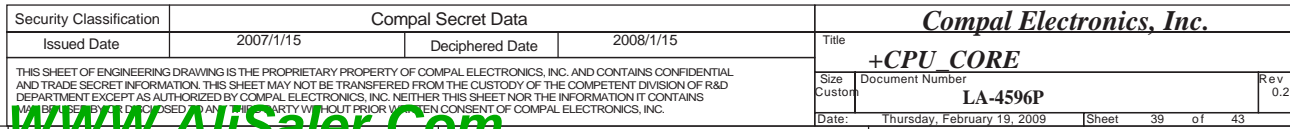


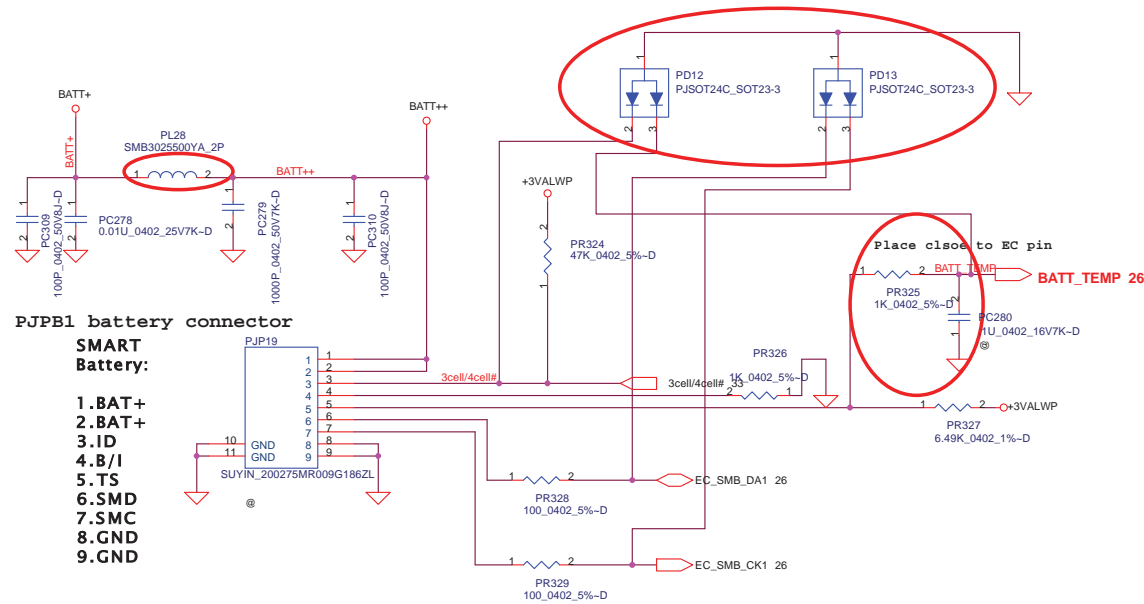
Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2006/10/1	Deciphered Date	2007/05/30	Title +1.8VP		
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				Date	Thursday, February 19, 2009	Sheet 36 of 43



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Issued Date	2008/2/5	Deciphered Date	2009/2/5	Title +1.5VSP		
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					LA-4596P	0.2
Date: Thursday, February 19, 2009				Sheet	37	of 43







B

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	32	DCIN /Vin Detector	08/12/08	COMPAL	common circuit design modify	change PR203 from 33 to 68 and add PR204 to 68	0.3
2			08/12/08	COMPAL	design modify	change PL17 from SM010018880 to SM010008E10	0.3
3	33	Charger	08/12/08	COMPAL	vendor FAE suggest	change PR272 PR339 from 1 to 3.3	0.3
4	40	BATTERY CONN	08/12/08	COMPAL	design modify	change PL28 from SM010018210 to SM010008E10	0.3
5	32	DCIN /Vin Detector	08/12/12	COMPAL	increase capacitor for EMI request	add PC313 at 0.01uf and PC314 at 0.1uf	0.3
6	35	VCCPP	08/12/12	COMPAL	change resister for EMI request	change PR342 from 0 to 2.2	0.3
7	36	1.8VP	08/12/12	COMPAL	change resister for EMI request	change PR352 from 0 to 2.2	0.3
8	37	1.5VSP	08/12/12	COMPAL	change resister for EMI request	change PR362 from 0 to 2.2	0.3
9							
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Issued Date	2007/1/15	Deciphered Date	2008/1/15	Title	
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Date:		Thursday, February 19, 2009	Sheet	41	of 43

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	28	USB/BT/ FP/ Felica/Camera	2008/12/02	Compal_HW	Small USB board no function	Modify Pin definition of JUSBP3	0.2
2	24	HDA-IDT_92HD81	2008/12/02	Compal_HW	R voice and L voice fail	Modify Pin definition of JSPK1	0.2
3	27	PWR_OK/ BTN/ KB / TP/TPM1.2	2008/12/02	Compal_HW	Switch function fail	Modify Pin definition of SW1	0.2
4	21	LAN-8111D	2008/12/16	Compal_HW	EMI LAN test fail	Add C1817-C1820 for LAN connector	0.2
5	23	Mini-Card/WWAN/Roboson	2008/12/16	Compal_HW	S5 wake on Wirlesslan fail	Add U89 to control wirless lan voltage	0.2
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